

IN THE UNITED STATES DISTRICT COURT  
FOR THE EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION

NETLIST, INC., ( CAUSE NO. 2:21-CV-463-JRG  
)  
Plaintiff, ( )  
vs. ( )  
SAMSUNG ELECTRONICS CO., LTD., ( )  
et al., ( ) MARSHALL, TEXAS  
( NOVEMBER 4, 2022  
Defendants. ) 9:00 A.M.

MARKMAN HEARING

BEFORE THE HONORABLE ROY PAYNE  
UNITED STATES MAGISTRATE JUDGE

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1 THE COURT: Good morning. Please be seated.

2 For the record, we're here for the claim construction  
3 hearing in Netlist versus Samsung, which is Case No. 2:21-463  
4 on our docket.

5 Would counsel state their appearances for the record?

6 MS. TRUELOVE: Good morning, Your Honor. Jennifer  
7 Truelove for Plaintiff Netlist. With me today and who will be  
8 presenting is Mr. Jason Sheasby, his colleague Annita Zhong,  
9 and Michael Tezyan. We also have with us today some corporate  
10 representatives, Jayson Sohi, Tobin Hobbs, and Jamie Zheng.  
11 We are ready to proceed.

12 THE COURT: All right. Thank you, Ms. Truelove.

13 MS. SMITH: Good morning, Your Honor. Melissa Smith  
14 on behalf of SamSUNG. I'm joined this morning by Mr. Mike  
15 McKeon, Mr. Matt Colvin, Dr. Frank Albert, Mr. Jeff Burton.  
16 And then, Your Honor, we also have two corporate  
17 representatives from Samsung today--Young-Jun Choi, as well as  
18 Won-Jin Lee. And Your Honor, we're ready to proceed.

19 THE COURT: All right. Thank you, Ms. Smith.

20 I will also point out for the record that earlier this  
21 morning we distributed to counsel for both sides a set of  
22 preliminary constructions of the disputed terms. The purpose  
23 of issuing those preliminary constructions is not to deter  
24 either side from taking whatever positions they think are  
25 appropriate on these terms; rather, the preliminary

1 constructions are designed to let you know where the Court is  
2 after the initial review of the briefing and the record so  
3 that you can focus your arguments where you think the Court  
4 may have most gone astray. I do reserve the right to amend  
5 these preliminary constructions, and not uncommonly do alter  
6 them based on the arguments received at this hearing, so I  
7 hope that you will take them in that spirit.

8 I'd like to hear the arguments on a term-by-term basis,  
9 but I'm happy to take them in whatever order counsel think is  
10 most productive and to group them if counsel think that would  
11 be efficient.

12 And I will note also that a variety of these preliminary  
13 constructions have notes on them. Those notes are not part of  
14 the official construction; they're designed to let you know  
15 what will be reflected in the order that issues so that even  
16 though it might say 'plain and ordinary meaning', there will  
17 be further discussion in the order that issues designed to  
18 govern the way the experts handle these terms. So I just  
19 wanted to let you know that's what those parenthetical notes  
20 are intended to communicate.

21 Having said that, I'll turn it over first to counsel for  
22 Plaintiff.

23 Good morning, Mr. Sheasby.

24 MR. SHEASBY: Good morning, Your Honor. May it  
25 please the Court.

1           On term A, we will stand on the papers because the Court  
2           has preliminarily adopted our construction, and perhaps  
3           Samsung would appreciate the opportunity to argue on that one.

4           THE COURT: All right.

5           MR. McKEON: Good morning. Mike McKeon for Samsung.  
6           Always a pleasure to appear before you.

7           So I do want to make just a few points on the first term,  
8           the 'dual buck converter' term. And one thing I want to  
9           emphasize, and maybe we didn't do as good a job in our brief  
10          as we should have in this, but this term 'dual buck converter'  
11          that appears in dependent claims, it shows here on slide 7 a  
12          depiction of what that physically looks like in the patent and  
13          it's depicted in figure 16.

14          This term is not a term of art--'dual buck converter'.  
15          'Buck converter' is. That's why no one's disputing that term.  
16          But 'dual buck converter' doesn't have a common, ordinary,  
17          understood meaning, and that's why, you know, we think it's  
18          appropriate in this case to look to the specification to get  
19          guidance on that. And when you do that, what you see here is  
20          in figure 16 and the corresponding description at column 29 of  
21          the patent, starting at line 46, which really defines and  
22          gives meaning to what this term, which has no understood  
23          meaning in the art, what it means in the context of the  
24          patent. And what we see here is that when we talk about the  
25          dual buck converter, we have these two voltages coming out.

1 No one, of course, disputes that. It's two voltages coming  
2 out. But one voltage that comes out is different, distinct  
3 from the other voltage comes out.

4 And the explanation here in the patent is -- again, at  
5 column 29, is that you have the 2.5 voltage coming out, and in  
6 the context of the embodiment, it's going to a particular  
7 device in the whole system, an isolation device; whereas, the  
8 second voltage is a reduced voltage, and that's going to the  
9 -- a separate and distinct device--FPGA. And so we have these  
10 two voltages coming out, but the voltages are different.

11 And, in fact, if we go to slide 9 here in our  
12 presentation, what we see here if you look at all the buck  
13 converters, they all actually have different values at the  
14 output. And why is that? Because the patent describes in  
15 quite detail that we want to drive different types of  
16 components in the system, and these different components are  
17 going to have different voltage requirements. And the logic  
18 here, Your Honor, is, Well, if I had two components that only  
19 needed 1.8 volts, well, then I just need one output of a buck  
20 converter that I can send to both of those components. So I  
21 don't need -- if I have a buck converter with a dual output,  
22 it would be superfluous, completely redundant, unnecessary to  
23 have them be the same voltage.

24 And we see the descriptions in the specification here at  
25 column 29, you know, quoting here at line 33, you know, "an

1 appropriate amount of powering for the various components."  
2 And the way the system is defined in the patent, and  
3 particularly the buck converters, in every instance -- there's  
4 not a single instance where we have a different value or a  
5 same value coming out not only within the dual buck converter,  
6 but actually across the buck converters, because again, that  
7 would be superfluous; you wouldn't need to do that.

8 One final point, Your Honor, is there is a claim in the  
9 patent where we talk about a first and third buck converters  
10 are configured to operate as a dual buck converter, and the  
11 point here is that when -- if I had these separate buck  
12 converters that had these separate values in the independent  
13 claim and I bring them together in the dependent claim, then  
14 they're going to have -- retain their separate values and --  
15 when they're combined as a dual buck converter. And again,  
16 it -- you know, it would make no sense as a matter of logic or  
17 as a matter of the technology as described in this patent to  
18 have them be the same value because you would just have one  
19 output then that would go to the different components.

20 THE COURT: You know, Mr. McKeon, that sounds like a  
21 good argument to me for the system having the capability to  
22 have a different value out of each buck converter, but where  
23 do you derive a requirement that it can only be different  
24 values?

25 MR. McKEON: I would say, Your Honor, when the

1 disclosure is limiting in that way, when THE -- to describe  
2 the embodiment -- and again, this is not a term of art. When  
3 they describe 'dual buck converter' in the patent, it's only  
4 described this way. And I do concede, Your Honor, looking at  
5 the claim language itself, you know, if you want to take the  
6 most broadest view of the claim language itself, your proposed  
7 construction in the preliminary is, you know, within that  
8 logic. But if you look at the specification and one of  
9 ordinary skill in the art is thinking, What about the dual  
10 buck converter, I'm going to have to go to the specification,  
11 and when you have it consistently and uniquely defined in this  
12 way, then, you know, we think that's limiting, and that's  
13 really the source of our point here, our argument here.

14 THE COURT: You know, I would quibble with your use  
15 of the word 'defined'. I don't see it defined in the  
16 specification at all.

17 MR. McKEON: What I would say, Your Honor, we rely  
18 on cases like *Bell Atlantic* where you have these -- you know,  
19 defined by implication. You're absolutely right, Your Honor;  
20 it's not defined in the sense that 'dual buck converter' is  
21 herein defined as X, Y, and Z, and that's definitely the case,  
22 Your Honor. But when you have a description of a component  
23 that has no ordinary meaning in the art and it's the only  
24 description of it, then you have to define it by implication,  
25 and we think that's really what's going on here in the context



1 of this term.

2 THE COURT: And let me back up and question a  
3 premise you have on the screen right now, which is that the  
4 first buck converter and the third buck converter must involve  
5 different voltage amplitudes. Is that just an implicit  
6 characteristic as you see it, or is there something in the  
7 specification that you think requires that?

8 MR. McKEON: Again, Your Honor, going back to the --  
9 sort of the main foundation of our argument, which is the only  
10 disclosure is that they have -- all have separate values  
11 coming out. And again, it would be superfluous if I was to  
12 have -- if these were all the same values, to be superfluous  
13 you would just need one output and you could drive as many  
14 different components in the system as you wanted to with that  
15 one value. The point is that these difference components that  
16 are in the system require different values.

17 And that is why we have these -- you know, you have these  
18 -- this one voltage coming into all these buck converters, you  
19 have one voltage coming in at 1110 or, alternatively, 1112.  
20 That's value coming in. One value is coming in. And these  
21 different buck converters are going to downscale that value,  
22 it's actually five volts coming in, and they're each going to  
23 down-tick the value to the appropriate level and they're all  
24 going to have different values. And if you had a system where  
25 they could be the same, then you wouldn't need these different

1 buck converters.

2 And we just think with the term 'dual buck converter',  
3 particularly because it's not defined in the art, you know,  
4 you're going to have to be stuck with you what you disclosed  
5 to the public in your patent. And that's the main point and  
6 premise of the argument, Your Honor.

7 THE COURT: All right. Thank you, Mr. McKeon.

8 MS. SMITH: Your Honor, may I pass up some slides,  
9 please?

10 THE COURT: Sure.

11 MS. SMITH: Thank you.

12 THE COURT: Thank you, Ms. Smith.

13 Go ahead Mr. Sheasby.

14 MR. SHEASBY: Thank you, Your Honor.

15 I think the basic premise of the argument is that two  
16 separate components cannot demand the same value on the  
17 module, and that is absolutely inconsistent with the patent.  
18 This is the '918 Patent, 29, 18 through 64, and this is an  
19 object lesson in why there may be lots of reasons to have  
20 separate circuits delivering the same voltage.

21 So in this example the DRAM, flash, and controller all  
22 require 1.8 volts, and there is an option of them being  
23 supplied over a single line, 1102. But then if you go down to  
24 the bottom of that same passage, it makes clear that an  
25 independent voltage can be used to supply the DRAM and flash.

1 And, of course, those DRAM and flashes still require the same  
2 1.8 volts; they're just being supplied independently. And so  
3 the basic premise that each of the wires has to, in effect,  
4 supply a different voltage is not in the specification itself.

5 The dual buck converter, there is no evidence that that's  
6 a specialized term of art or a term that was coined by the  
7 patent owner in this case. The purpose of the figure 16  
8 embodiment is to note that you can use lots of different types  
9 of power management tools. You can use buck converters, you  
10 can use dual buck converters, you can use buck and burst  
11 converters, but there's no requirement or -- there's no  
12 requirement or standard that each of those has to deliver a  
13 different voltage. For example, we know in the preferred  
14 embodiment that the voltage 1122 is outputting 1.8 volts, but,  
15 in the alternative, there can be a separate for DRAMs, flash,  
16 and FPGA, but we know in the alternative embodiment there  
17 could be an independent voltage.

18 Thank you, Your Honor.

19 THE COURT: And Mr. Sheasby, is there a reason that  
20 you can articulate why a dual buck converter would have the  
21 same voltage coming out on both lines?

22 MR. SHEASBY: There is, Your Honor, and I can  
23 explain it. There is two reasons.

24 If you go to slide 66.

25 In particular in FPGA--and you can look at this from the

1 specification itself--the FPGA operates not just at one  
2 voltage; it can operate at multiple voltages at different  
3 particular times. And that's talked about in the  
4 specification. If you ran the core of the FPGA, you would  
5 operate at one voltage; if you ran other elements of the FPGA,  
6 you'd operate at another voltage. And so, for example, this  
7 is talking about FPGAs that operate across voltage ranges that  
8 start from 1 and go up to 2.5 volts.

9 And so the reason for the dual buck converter having the  
10 capability of doing different voltages, but not requirement,  
11 is that it's not an assumption that the voltage demand for a  
12 given component will stay the same throughout the operating  
13 cycle. And the specification in particular talks about the  
14 FPGA operating at different voltages in different events.

15 THE COURT: All right.

16 MR. SHEASBY: Thank you, Your Honor.

17 THE COURT: Thank you, Mr. Sheasby.

18 MR. McKEON: Your Honor, I think you got the  
19 argument, so with that, we rest.

20 THE COURT: All right, then. Thank you, Mr. McKeon.

21 And we can take the next term.

22 MR. SHEASBY: Your Honor, I think for B, C, and D we  
23 will stand on our briefing.

24 THE COURT: All right.

25 MR. McKEON: Ms. Andrews, can we have the slides?

1 All right. 'Pre-regulated input voltage', Your Honor.  
2 So, I mean, the dispute here, of course, as Your Honor knows  
3 reviewing the briefs is, you know, whether this regulated  
4 voltage needs to be generated on the memory module itself.  
5 That's really the crux of the dispute here. And, you know,  
6 I'll note that their proposal, of course, modulated input  
7 voltage. And the thing about their proposal, Your Honor, it  
8 takes out the word 'pre-regulated'. 'Pre-regulated' must mean  
9 something. You know, 'pre-regulated input voltage'. And if  
10 you just say 'modulated input voltage', what does that -- that  
11 really changes the character of what 'pre-regulated input  
12 voltage' is.

13 And we think from the context of the disclosure in the  
14 patent, and also the claims, is that the pre-regulated  
15 voltage, it comes from the input voltage, the source of it,  
16 but the key is that it's actually done on the module. And, of  
17 course, the pre-regulated voltages serve to be an input into  
18 the buck converters we just talked about.

19 And this is where the language appears in the claim. And  
20 just take a second, Your Honor, if I can, to walk through --  
21 sort of piece together how the claim operates in these  
22 different elements. Of course, we have that printed circuit  
23 board. And we had this input voltage. That comes in and that  
24 is going to this power element. And the power element is what  
25 is generating on the actual module, on the circuit board, it's

1 generating the pre-regulated input voltage which, in turn,  
2 goes to the buck converters and, of course, is an output and  
3 that goes to another component. So the patent is very clear  
4 in its description how these all relate, and we -- you know,  
5 we think the claim is very consistent with that.

6 And the disclosure here, Your Honor, is also very clear  
7 on this. And what we've highlighted here in this red, these  
8 are the two power elements, and both take that input in and  
9 what they're doing is they're cranking that up to a higher  
10 level and they're pre-regulating the voltage. And what are  
11 they pre-regulating the voltage for? Well, they're  
12 pre-regulating it to be inputs into the buck converters we  
13 talked about. And then the buck converters, in turn, will  
14 down -- you know, down shift the voltage. But the  
15 pre-regulated voltage is something that's generated on the  
16 power module because it's tied directly to the buck  
17 converters. They're the inputs to the buck converters. And,  
18 of course, we see that in the disclosure how they're all tied  
19 together.

20 Now, there's an argument made by our capable counsel  
21 here on the other side about figure 12, and I just want to  
22 quickly respond to that. Now, figure 12 is a different  
23 configuration, and then what I have here on the slide is  
24 figure 12 and this power source 1080. And the argument that  
25 was made is, Well, what if you take the figure 12 power source

1 and you could bring it into figure 16. And there is  
2 disclosure in the patent that says that, but it has nothing to  
3 do with the pre-regulation. I mean, the figure 12 doesn't  
4 even talk about pre-regulated voltage.

5 And the reason why counsel points out figure 12 is  
6 because there is actually a section in connection with  
7 describing figure 12 that says 1080, this power source, can be  
8 off the module. It says that for figure 12. And they cite to  
9 that and say, Okay, Your Honor, therefore, you shouldn't have  
10 that requirement. But Your Honor, I think the point there is  
11 that actually the fact that it says it for figure 12 and does  
12 not say it for figure 16 I think is quite telling. I mean,  
13 they -- when they want to have clarity around where these  
14 different components could be and where these signals are  
15 generated, they gave you the option of figure 12, but they  
16 specifically did not do that in figure 16.

17 And figure 16, of course, is very important because  
18 that's where the pre-regulated voltage term is applicable.  
19 The pre-regulated voltage is the green here on the right, and  
20 that's coming from the power sources, and it's generated on  
21 the board, and it's tied directly to the buck converters. And  
22 the way they've construed it, Your Honor, and I fear the way  
23 that your preliminary -- the scope of your preliminary is  
24 that, you know, this pre-regulated voltage can be generated,  
25 you know, systems away, and as long as it ends up into the

1 buck converters that's all that matters. And we just think,  
2 Your Honor, that's a step too far given the context of this  
3 term as it's used in the patent, and also, you know, the  
4 pre-regulation. That's a term in the claim. And I fear, Your  
5 Honor, that your construction just removes that. And what  
6 meaning does that have in the context of this claim and this  
7 patent--pre-regulated voltage. And we feel, Your Honor, that,  
8 you know, it's got to be tied directly to those buck  
9 converters and it's got to be generated on the module.

10 And with that, Your Honor, I'll save --

11 THE COURT: I guess my initial read on this is that  
12 while pre-regulated voltage is a limitation of the claim that  
13 has to be met, the claim as it's written is agnostic as to  
14 where that occurs. And I understand that there is an  
15 embodiment which is displayed in figure 16 that would support  
16 your understanding of it, but my difficulty is in finding that  
17 that embodiment has to be read into the claim.

18 MR. McKEON: And Your Honor, that's obviously a  
19 great question, and what I would say to that is, you know,  
20 again, I would just -- I would hang my hooks onto that  
21 'pre-regulated' term. But if you look at the way the claims  
22 set up, you've got this input voltage coming in and it's  
23 coming in from these edge connections, and the edge  
24 connections are on the module. So I have the input voltage  
25 coming from the edge connections and then I'm generating these



1 pre-regulated input voltages. They're pre-regulated input  
2 voltages, and these input voltages, where do they come from?  
3 They don't just fall from the sky. They came in through the  
4 edge connection. So the input voltages are on the board. And  
5 when they make the pre-regulated input voltages, I'm doing  
6 that on the board because they're coming from what came in  
7 through the edge connection.

8 So I think the claim itself really gives you the  
9 structure of how these voltages are related, and it's tied  
10 directly back to figure 16. So they're coming in from the  
11 edge. That's a structural limitation there. The input  
12 voltages are coming into the edge, and then they go into the  
13 power circuit, and they are pre-regulated, and that's all on  
14 the board. And, you know, the pre-regulated input voltages,  
15 again, they are not just falling from the sky; they're coming  
16 -- they're generated on the board, and the source of them, you  
17 know, is what's coming into those edge connections. That's  
18 the source of that power. And so the claim itself is what  
19 really puts that structure together there, and I think, you  
20 know, when you look at the patent it really brings it home.

21 THE COURT: All right.

22 MR. McKEON: Thank you, Your Honor.

23 THE COURT: Thank you, Mr. McKeon.

24 MS. ZHONG: Can we switch? Thank you very much.

25 THE COURT: And Ms. Zhong, if you can pull that mic

1 down to you. I want to make sure I can hear you. Thank you.

2 MS. ZHONG: Can you hear me now?

3 THE COURT: Yes.

4 MS. ZHONG: Thank you, Your Honor.

5 So why don't we start with slide No. 72.

6 Let's start with the claim language. And Your Honor has  
7 pointed out there is really no connection between the  
8 pre-regulated input voltage and the input voltage that's  
9 received from the edge connection. As Samsung's counsel has  
10 pointed out, the pre-regulated input voltage is an input for  
11 the buck converters, and there is a separate input voltage  
12 from the portion received at the edge connections. The claim  
13 otherwise does not place any restrictions on the two terms.

14 And then if we go to figure 16 that the counsel has hang  
15 its hat on, if you look at figure 16, it's not a memory  
16 module. What it says is a power module. The power module can  
17 be part of the memory module or it can be off the memory  
18 module. So think about when it's off the module there is a  
19 memory module, there is a separate connector where the power  
20 module is actually connected to the memory module. So figure  
21 16, the caption of it, the description in column 9, lines 39  
22 to 41, says figure 16 is a power module illustrating a power  
23 module. It's not illustrating the memory module. That power  
24 module can be part of the memory module as shown in, for  
25 example, figure 12, 13, and 14 illustrated on the same PCB, or

1 as described in the specification for figure 12, it can be off  
2 module.

3 So Your Honor got it right--the pre-regulated voltage  
4 need not be generated on the same PCB as the memory. They can  
5 be off module. The patent the inventors anticipated and  
6 described both possibilities, and that's in, for example,  
7 column 26, lines 26 through 35.

8 So in column 26 through 35, they contemplated both having  
9 the second power module 1080 on the same PCB as a memory  
10 module as the rest of the memory or it's to be off. And the  
11 power module is exactly the same.

12 If Your Honor doesn't have any additional questions, we  
13 will rest on the paper at this time.

14 THE COURT: All right. Thank you, Ms. Zhong.

15 MR. McKEON: Your Honor, a quick response to that?

16 THE COURT: Certainly.

17 MR. McKEON: And again, Your Honor, I just want to  
18 emphasize, the description regarding having the power module,  
19 you know, removed from the memory module, that's in column 26  
20 with connection with figure 12, and then -- and counsel cited  
21 that, you know, being at line 30. And the point is that  
22 description does not appear anywhere in connection with figure  
23 16, and the claims here are clearly directed at figure 16. If  
24 you're talking about buck converters and all that, that's  
25 figure 16. That's -- the only disclosure of the system is

1 figure 16. And the fact that that same description that  
2 counsel pointed to is not anywhere near figure 16 description  
3 really tells -- I think tells the reader and one of ordinary  
4 skill in the art that this is a different configuration of  
5 figure 12. And with respect to figure 16 description, what  
6 the claim corresponds to, these are done on the module. And  
7 again, the word -- the 'pre-regulated' language I think  
8 supports that.

9 With that, Your Honor, unless you have any questions, we  
10 can turn to the next term.

11 THE COURT: All right. Thank you, Mr. McKeon.

12 MR. SHEASBY: Mr. McKeon, I already said I was going  
13 to rest on -- just to make it more efficient, the next three  
14 I'm going to rest on.

15 MR. McKEON: Thank you.

16 THE COURT: All right. So I'll hear from the  
17 Defendant on anything on the C and D terms.

18 MR. McKEON: Thank you.

19 On this one, Your Honor, if I may -- so 'first',  
20 'second', 'third', and 'fourth'. And I think the issue here,  
21 Your Honor, is what is 'distinct'. And as Your Honor -- you  
22 know, the case law is clear that, you know, these need to be  
23 distinct. So we're having an issue about what is 'distinct'.  
24 And I think, you know, were -- the construction, as Your Honor  
25 put in the preliminary, 'distinct' is just physically

1 separate; it's distinct, and in our -- we're going further  
2 than that; we're saying yes, you've got to have that, but you  
3 also -- in the context of this patent and this art, 'distinct'  
4 also needs to be distinct in value. So, you know, separate  
5 and then distinct in terms of the values.

6 And on this point, Your Honor, there's a case  
7 *Alexsam/Cigna* case that we cite in the brief, and the issue  
8 there was the first database distinct from the second  
9 database. And this is one of your decisions, Your Honor. And  
10 what you held there, you know, you held they have to be  
11 distinct consistent with the case law, but then you said, you  
12 know, you're not going to get into the issue about what that  
13 means in the context of that dispute. You felt that was  
14 something the jury should decide. And what we would invite  
15 here, Your Honor, is this same result. Let 'distinct' -- we  
16 all agree they have to be distinct, and there's no dispute  
17 about that. And what we would invite, Your Honor, is sort of  
18 following the logic of the *Alexsam* case and let's let the jury  
19 decide the context of this patent and technology--you know,  
20 what does it mean to be distinct. And I think that's  
21 something that our experts are going to get up there and talk  
22 about and that's something that the jury can ultimately decide  
23 in the context of this technology and this patent.

24 THE COURT: You know, in the *Alexsam* case, what we  
25 were concerned about was the issue there you have a single

1 database and one side wants to draw lines and partition it  
2 into allegedly multiple databases, and that was the fact issue  
3 that was involved with whether they were distinct. I don't  
4 see that there's a similar issue here with these first through  
5 fourth voltages, but --

6 MR. McKEON: Yeah. I mean, I guess, Your Honor, the  
7 -- I mean, I would say the logic applies equally and, you  
8 know, so I get the line-drawing point is it a distinct debate  
9 as different in nature, but fundamentally, you know, whether  
10 the voltages first, second, and third are distinct in the  
11 context of this technology, you know, ultimately that's the  
12 question at hand here, and I think that was -- I think that's  
13 best left to the jury in this context, following the same  
14 logic.

15 THE COURT: Well, I just wanted to make sure that it  
16 was clear that the position that I'm taking at this point is  
17 that you are right, they have to be distinct, but I'm not  
18 agreeing that being distinct means they have to have different  
19 amplitudes, and that's what I guess to a certain extent you  
20 were talking about before. I understand that may be the  
21 highest and best use of this system, but the question is do  
22 the claims require it, and that's what I'm struggling with.

23 MR. McKEON: Yeah. And I -- that is certainly the  
24 debate, Your Honor, and that's why, you know, I invite the  
25 Court to, you know, use the same logic that you did in the

1     *Alexsam* case here and let the jury decide whether in this  
2     context what we see here on slide 16 and whether these are  
3     distinct, you know, in the context of an accused system or  
4     not, and let that just -- the jury decide that ultimately, and  
5     leave it at distinct, that will be part of the construction,  
6     and then the jury can take it from there.

7             THE COURT: All right. I understand the argument.

8             MR. McKEON: Thank you, Your Honor.

9             THE COURT: Thank you, Mr. McKeon.

10            MR. SHEASBY: So we start with the claim language  
11     the Federal Circuit requires. If you look at the claims, it  
12     recites one or more regulated voltages, so multiple regulated  
13     voltages through the fourth. And then -- that's claim 23 of  
14     the '918. And then in dependent claim 29 it makes clear that  
15     those regulated voltages can actually have the same amount.

16            THE COURT: Mr. Sheasby, you're a bit taller than  
17     your co-counsel. If you could adjust that mic that would  
18     help. Thank you.

19            MR. SHEASBY: Not in personality, Your Honor; only  
20     in height.

21            You asked this question, which is why would two separate  
22     lines give the same voltage, and I gave you one example from  
23     the specification that the FPGA operates in different states  
24     and, therefore, requires different voltages. There's another  
25     example. So if you look at this specification '918, 29, 18

1 through 64, it talks about the wire, the rail for the voltage  
2 being provided at 1.8 volts for two amps for 60 seconds. And,  
3 of course, what we know from electrical engineering is that  
4 voltage is only one aspect of what triggers the load that's  
5 placed on a circuit.

6 So the analogy that Doctor Zhong gave to me yesterday was  
7 the following: There's a reason why you don't plug in a power  
8 strip and plug in four microwaves all at 110 volts into the  
9 same circuit, and the reason for that is that you'll short the  
10 circuit because the load will be too great. And what this  
11 passage is speaking about is the fact that one circuit--this  
12 is 1122--is going to provide 1.8 volts, but it's going to  
13 provide it two amps for 60 seconds. But you may need the same  
14 voltage but different amps and a different load for another  
15 circuit, and that's why the specification expressly describes  
16 the voltages as being able to be independent even though  
17 they're the same amount, because voltage is only one of the  
18 three parameters that describe how you feed the modules that  
19 you're dealing where.

20 If you go to slide 57.

21 This is another example that we look at. This is  
22 from --

23 Slide 56.

24 This is from PNC -- from Samsung's own papers. This is  
25 Exhibit 30 to our reply at papers 15 and 30. And they



1 acknowledge this as well, that separate voltages can have the  
2 same amplitudes.

3 So this is I don't think anything esoteric or funny.  
4 This is a basic element of electrical engineering, which is  
5 that you may want different rails or different pipes all  
6 differing the same voltages because voltage is only one of the  
7 parameters that is contributing to the load you need to feed  
8 from those circuits.

9 I'll rest on that, Your Honor, unless you have any  
10 questions.

11 THE COURT: All right. Thank you, Mr. Sheasby.

12 MR. SHEASBY: Thank you, Your Honor.

13 MR. McKEON: Just a brief response, Your Honor?

14 THE COURT: Certainly.

15 MR. McKEON: Just for the record, and we do take  
16 issue with the description that the specification discloses  
17 using the same voltage in these different components and, you  
18 know, Mr. Sheasby pointed to some extrinsic evidence Samsung  
19 documents regarding how their systems -- well, I guess it's a  
20 JESD bag. But the point is in the specification there's no  
21 disclosure of that in the specification.

22 THE COURT: Well, I guess the question is, what I  
23 understand from the Plaintiff's argument is that they're  
24 saying that's a reason why it would make sense for the  
25 capability to have different voltages but not a requirement.

1 And if you want to rebut the argument that it would be useful  
2 to be able to have the same voltages from the different  
3 circuits, then tell me about it, but that is what I'm  
4 struggling with--just because the embodiment shows separate  
5 voltages, does that make it a limitation.

6 MR. McKEON: And I would say yes, Your Honor, in  
7 this context. I mean, again, there is just no disclosure  
8 where you have it -- they'd have the -- they would be the  
9 same. And then, of course, in the context of the patent,  
10 where you have these various buck converters, they're going to  
11 different places, and there's no disclosure that you would  
12 have -- that a particular FPGA in one system would have the  
13 same voltage as an FPGA in another part of the system.  
14 There's no disclosure on that. And yes, you can have  
15 different FPGAs, but there's no disclosure that they would  
16 necessarily have the same voltage.

17 And maybe in a real-world system you would have  
18 situations where that would be the case, but we're limited to  
19 what we've got here in the patent documents. And when you  
20 have this disclosure that's very specific in terms of the  
21 different values of these signals and nothing else, then, you  
22 know, we think that's limiting.

23 THE COURT: All right. I do understand the  
24 argument. Thank you.

25 MR. McKEON: Thank you, Your Honor.

1 MR. SHEASBY: Your Honor, we'll rest on -- I think I  
2 just referred Your Honor to the passage 29, 33 through 64  
3 which talks about a flash and DRAM, two separate components  
4 both at 1.8 volts, and we disclosed them being fed by separate  
5 independent lines.

6 And with that, as to term E we'll rest as well, if my  
7 brother would like to argue that in the first instance.

8 Term E. Did you want to argue term E?

9 MR. McKEON: Your Honor, we're going to rest for D,  
10 E, and F. We will rest on the papers.

11 MR. SHEASBY: So with Your Honor's permission, we  
12 will argue F.

13 THE COURT: All right. Go ahead.

14 MR. SHEASBY: Thank you, Your Honor.

15 MS. ZHONG: Slide No. 80, please.

16 It's our position that the memory module should be  
17 limiting because it provides the antecedent basis for the test  
18 in the body. That's consistent throughout the claims. For  
19 example, claim No. 1, the preamble says a memory module, and  
20 that provides the antecedent basis for the end of the memory  
21 module at the end of the first limitation. There is  
22 well-established case law that says if the -- a term that's  
23 appearing in the preamble provides the antecedent basis for  
24 the text in the body, then that particular phrase should be  
25 considered unlimiting.

1 And with that I will rest.

2 THE COURT: You know, it can be limiting because it  
3 provides antecedent basis, but this certainly looks like  
4 nothing more than a statement of an intended use of the  
5 device. Does it provide any other meaning to it other than  
6 the intended use?

7 MS. ZHONG: Well, it requires -- if Your Honor looks  
8 at --

9 Let's go back to claim No. -- slide 81.

10 The first limitation is, A printed circuit board having  
11 interface configured to fit into a slot, and that interface is  
12 required to include a plurality of edge connections, to couple  
13 power, data, address and control signals between the memory  
14 module and the host system. So that provides a context.

15 There is an interface -- think about the DEM. There is a  
16 bunch of gold fingers on the edge. And that gold edge, those  
17 gold fingers are supposed to provide power data and control  
18 signals between the host and that memory module, like the DEM  
19 board. So it provides a context of it--what is that interface  
20 coupling. So the memory module provides that context. It's  
21 not an intended use. It provides -- defines a physical  
22 structure where the interface needs to couple the signals  
23 with.

24 THE COURT: So you're saying without the preamble  
25 being limiting, it does not -- the claim does not define a

1 complete apparatus?

2 MS. ZHONG: Well, it makes clear that the printed  
3 circuit board -- the interface on that printed circuit board  
4 is providing the -- is coupling the signals between the host  
5 and that system. So everything else -- for example, the  
6 voltage conversion, the plurality of the component coupled to  
7 that is part of the memory module between which -- and the  
8 host system the interface is providing the conduit, or like  
9 the pass way for the signals. So it does provide the context.

10 THE COURT: So you're saying that if we don't  
11 construe the preamble as limiting, the claim will not be  
12 clear as to what the -- whether the device is the memory  
13 module that's referred to at the end of the first limitation?

14 MS. ZHONG: That's correct. For example, whether  
15 the voltage conversion circuit needs to be part of the memory  
16 module or not, then it's not going to be clear.

17 THE COURT: All right. Thank you, Ms. Zhong.

18 MR. McKEON: Okay. All right. So Your Honor, just  
19 where you started, I mean, this really is intended use. The  
20 point is here you have this printed circuit board, and the  
21 printed circuit board is doing various things and it's just  
22 doing this coupling between these other things. These other  
23 things aren't part of -- it doesn't indicate here specifically  
24 that they're part of what the printed circuit board is doing.

25 And I think the case that we think is on point here, Your

1 Honor, is, you know, your ruling in the *Sol IP* case where we  
2 had the same situation where we had a reference to the  
3 wireless communication system that was in the preamble, and  
4 Your Honor, you know, the same logic really that applies here  
5 is that it really doesn't overcome that presumption that, you  
6 know, it's not limiting. And you don't -- it's not really  
7 part of the claim and part of the system that's claimed. Even  
8 though it is, in fact, referenced, you know, within the body  
9 of the claim, it's not really doing anything, and particularly  
10 in the case we have here which is really an intended use  
11 situation.

12 THE COURT: Well, the argument I'm hearing from the  
13 Plaintiff is that it may not be clear that the memory module  
14 identified at the end of the first limitation is the device  
15 itself, the claimed device. Do you believe that it is clear  
16 that the memory module within the first limitation is the  
17 overall device even if the preamble is not limiting?

18 MR. McKEON: Well, I think what's required is that  
19 the printed circuit board do these things. Right? It has the  
20 plurality of edge connections configured to couple power,  
21 data, and address and control signals. And the point there is  
22 the coupling that it's performing, this thing you hold in your  
23 hand, the coupling it's performing is between the memory  
24 module and the host system.

25 And, you know, the host system here has no antecedent

1 either. I mean, it doesn't --- I mean, that particular term  
2 doesn't have any antecedent. The point, though, is -- well, I  
3 guess it does. I take that back, Your Honor. It's up in the  
4 other -- in the top here.

5 But the point is that these two separate modules and the  
6 system for the host system, they're outside of what we're  
7 talking about here. And the only thing that the printed  
8 circuit board is doing, it's making sure that these power,  
9 data, address and control signals, that it's coupling between  
10 these two systems. And so I don't --

11 THE COURT: Well, the PCB that's claimed in the  
12 first limitation is claimed as part of the memory module,  
13 isn't it?

14 MR. McKEON: Well, it's a comprising term. Right?  
15 So it would include -- you know, it would include memory --  
16 the memory module will have a PCB, a voltage conversion  
17 circuit, and a plurality of components. That's how you'd read  
18 the claim, for sure.

19 THE COURT: Well, I guess what I'm hearing from the  
20 Plaintiff is the concern that if the preamble is not limiting,  
21 that first limitation could be read as referring to a memory  
22 module that is not part of the device that's claimed; that it  
23 is just referring to a connection between some unclaimed  
24 device, the memory module, and the host system.

25 MR. McKEON: I -- yeah, Your Honor. I don't -- I

1     guess I don't agree with the argument. I mean, the point is  
2     here you have the memory module, and it's not like the  
3     antecedent goes away and is irrelevant. You know, it still  
4     guides your -- how this claim operates. It's clearly -- the  
5     memory module that is at issue here is the one that the  
6     printed circuit board is sitting on, but doesn't mean -- it  
7     doesn't mean that all of the sudden the memory module is a  
8     requirement of the claim. It's just saying that between the  
9     memory module that the printed circuit board is sitting on and  
10    the host system, that's where these -- this connection is  
11    occurring, between those two things.

12           THE COURT: What difference do you see it would make  
13    if we construe the preamble as limiting?

14           MR. McKEON: Well, I mean, in terms of how it  
15    impacts the case, Your Honor, I -- you know, it's not clear  
16    the scope of the impact that it would have. But, you know,  
17    for just ordinary rules of claim construction here, I think  
18    this is a situation where we wouldn't want that to be limiting  
19    based on the fact that this is really, you know, an intended  
20    use situation. And despite the fact that the memory module is  
21    referenced in the text of the body of the claim, you know,  
22    it's not limiting in the context here.

23           THE COURT: I guess what I'm going to have to figure  
24    out is whether I think that the preamble gives life or meaning  
25    to the claim in view of the argument that the memory module in



1 the limitation could be understood to be something other than  
2 the claimed device. But anyway, I'll -- I will look at that  
3 further.

4 MR. McKEON: Okay. Thank you, Your Honor.

5 THE COURT: Thank you, Mr. McKeon.

6 MS. ZHONG: Your Honor, just one clarification. The  
7 reason we want to make sure that the memory module is limiting  
8 is to make sure that each of the claimed elements, printed  
9 circuit board, voltage conversion circuit, and a plurality of  
10 the components, we want to make sure these are all part of the  
11 memory module. Without that, there could be confusion. And  
12 it doesn't seem that Samsung's counsel disagrees with it. We  
13 want that. We just want the clarity so there is no argument  
14 down the road.

15 THE COURT: All right. I understand that position.  
16 Thank you.

17 That takes us to the 'array die' term.

18 And I can tell you, Mr. Sheasby, that the basis of this  
19 construction is the prosecution history disclaimer argument,  
20 in case that wasn't clear.

21 MR. SHEASBY: Understood, Your Honor. And let me go  
22 straight there.

23 So this is the passage from the prosecution history, and  
24 it does, indeed, say that Rajan merely discloses DRAM circuits  
25 206A through D, which are different from the array dies. And

1 I understand that Your Honor has concluded that that is a  
2 disclaimer. The issue that I have is that -- we understand  
3 that -- does Your Honor intend to give anymore guidance as to  
4 what the DRAM circuits are that is excluded, or will that be  
5 for the experts to analyze?

6 THE COURT: That would be for the experts. I do not  
7 intend to try and define what DRAM circuits that are  
8 disclaimed.

9 MR. SHEASBY: I understand, Your Honor.

10 With that clarification, there's no need for any  
11 additional argument. Thank you, Your Honor.

12 THE COURT: All right. Thank you.

13 MR. COLVIN: Your Honor, Samsung will rest on the  
14 papers for that term as well.

15 THE COURT: All right. Thank you, Mr. Colvin.

16 MR. SHEASBY: Your Honor, we will rest as to H on  
17 the papers.

18 THE COURT: All right.

19 MR. COLVIN: Samsung will also rest on the papers,  
20 Your Honor.

21 THE COURT: Thank you, Mr. Colvin.

22 MR. SHEASBY: And I believe that I, J, and K are all  
23 the adoption of our positions, and so if Samsung wants to  
24 argue those I'll allow them, obviously. So we don't have to  
25 jump up so often. I won't allow you to do anything. You can

1 do whatever you want. My point is that I won't sit up here,  
2 and let you guys do what you want.

3 THE COURT: All right.

4 Doctor Albert.

5 DOCTOR ALBERT: Good morning, Your Honor. Frank  
6 Albert for Samsung.

7 The first term here, term I, 'before receiving the input  
8 C/A signals corresponding to the memory read operation', and  
9 Samsung's proposed construction is 'during one or more  
10 previous memory operations'. What we believe is this provides  
11 clarity to the term, it is based on admissions made by Netlist  
12 during the prosecution, as well as the clarity provided by the  
13 specification.

14 Let's take a look at the claim here. So the highlighted  
15 portion here is the actual claim language that we're  
16 discussing, 'before receiving the input C/A signals  
17 corresponding to the memory read operations at the module  
18 control device'. It's 'before receiving' that is the thrust  
19 of the attention here. That portion of the claim relates back  
20 to an earlier part of the claim, 'receiving at the module  
21 control device input C/A signals corresponding to the memory  
22 read operation'.

23 The second half of the construction, the thrust of the  
24 discussion here is determining the first pre-determined amount  
25 based at least on signals received at the first data buffer.

1 So really the question is when is it linked between -- when is  
2 it that determining the pre-determined amount, when does it  
3 actually happen; what does 'before receiving the input signals  
4 corresponding to the memory read operation at the memory  
5 module' mean in the context of this claim, this patent, this  
6 prosecution history.

7 So if you look to the patent, figure 18 provides a good  
8 illustration of that. We start off with steps 1810 and 1820.  
9 There's a previous write operation. You can see that in  
10 1820--'receiving a write strobe signal'. And then based on  
11 that previous memory operation, a pre-determined amount of  
12 delay is generated. It says right there in 1830, 'generating  
13 a delay signal according to the time interval'.

14 Now, later on when we receive a read signal in 1860 and  
15 1870, that read signal, there's going to be a delay in the  
16 read strobe here at 1880 based on that pre-determined amount  
17 that was determined earlier during that previous memory  
18 operation.

19 Now, if you look to the specification, over and over and  
20 over again is the determining that pre-determined amount  
21 that's linked to that previous memory operation. Here we have  
22 some examples. Patent -- '506 Patent at 4, 9 to 19, single  
23 alignment circuits that determine during the write operation  
24 the time interval. Again, the time interval is used during  
25 subsequent read operation to time transmission of the read

1 data to the memory controller. Another example --

2 THE COURT: Mr. Albert, the passage that you just  
3 read starts with "Further, in one embodiment". Why should I  
4 take that as a limitation?

5 DOCTOR ALBERT: It's not just this embodiment, Your  
6 Honor. It's over and over and over again in the patent. And  
7 if you look to the prosecution history as well, they actually  
8 explain, further explain what this means. So let me -- I  
9 could fly by these other slides, Your Honor. These are just  
10 additional examples of time and time again where the patent  
11 talks about determining that time, that delay time based on  
12 the prior write operation, prior memory operation. And Your  
13 Honor is very familiar with, you know, the law on consistent  
14 description in the specification helping to construe the  
15 patent and the claim terms.

16 I mentioned the prosecution history, Your Honor, and  
17 here's what I'm getting at. There were claims that were  
18 allowed--claim 2 is an example of that--where the allowed  
19 subject matter read before the memory read operation; very  
20 similar to the language that we have here--before the memory  
21 read operation. And there was notice of allowance. Claims  
22 were going to issue. After that notice of allowance, the  
23 patentee went back to the Patent Office and changed the claim  
24 language, changed 'before the memory read operation' to  
25 'during one or more previous operations'. It did that for

1 claim 2, 3, 4, 5; did it over and over and over and over  
2 again.

3 And in the remarks corresponding to that amendment, the  
4 patentee said that this change, this changing from--I'll go  
5 back--'before the memory read operation' to 'during one or  
6 more previous operations', that's not a big change. It said  
7 specifically, "...have been amended to address minor issues of  
8 clarity and correct grammatical errors. No new matter has  
9 been added." The patentee there is saying that these two  
10 terms, they mean the same thing.

11 THE COURT: And, of course, we're not construing  
12 either of those terms.

13 DOCTOR ALBERT: And I will get to that, Your Honor.  
14 Very good question. I had that very same question when I was  
15 going through these materials myself.

16 And just to go back to the amendment, of course, the --  
17 this change wasn't changing the scope because the Patent  
18 Office doesn't allow that. The rules for patent examination  
19 say that you can make a post-allowance amendment, but you  
20 can't change the scope. So we know that the Patent Office  
21 determined that the scope for this change would have been  
22 equivalent.

23 Now, we're talking about one or more previous memory  
24 operations versus one or more previous operations. Now,  
25 Netlist in this case, that was one of the terms that we were

1 seeking to construe. There actually is an agreement for this  
2 patent, "'one or more previous operations' means 'one or more  
3 previous memory operations'."

4 So getting to Your Honor's question, the claim language  
5 that we're seeking to construe here, and I'll come back to it,  
6 'before receiving the input C/A signals corresponding'--again,  
7 these are corresponding to the memory read operation. Again,  
8 going back to that prosecution history, the memory read  
9 operation -- 'before the memory read operation' was equivalent  
10 to 'during one or more previous memory operations'.

11 So we have equivalent language here in the claim 'before  
12 receiving the input C/A signals corresponding to the memory  
13 read operation' when Netlist has already agreed to the Patent  
14 Office that before--I'll just go back to it--"'before the  
15 memory read operation' means 'during one or more previous  
16 operations'," which in this case Netlist has agreed in -- you  
17 see this in the joint claim construction chart "'one or more  
18 previous operations' means 'one or more previous memory  
19 operations'."

20 And so with that, Your Honor, I will pass the podium  
21 unless Your Honor has any questions.

22 THE COURT: Doesn't that equivalence depend on the  
23 context of each claim? I mean, to the extent that there's an  
24 agreement, isn't it an agreement that in those claims the  
25 claim scope wasn't altered by the different language?

1 DOCTOR ALBERT: Well, we can go back to the claim  
2 language itself that was purported to be equivalence, to  
3 answer your question. "'Before the memory read operation' is  
4 replaced with 'during one or more previous operations'."  
5 Again, the language that is being swapped out as equivalent  
6 starts with that memory operation.

7 THE COURT: What is there that is unclear about the  
8 language that you're seeking to construe? It seems very  
9 specific to me.

10 DOCTOR ALBERT: Yes, Your Honor.

11 So the ambiguity here is when this time interval is  
12 determined. And here the patent is very clear that that time  
13 interval is determined during a previous memory operation. We  
14 see it time and time and time again. And then in the  
15 prosecution history the two terms are equated as equivalence.

16 So we believe there should be no ambiguity; but to the  
17 extent Netlist wants to come in here and claim that's not what  
18 this means, that it means something else, then we would take  
19 issue with that.

20 THE COURT: All right. Thank you.

21 DOCTOR ALBERT: Thank you, Your Honor.

22 MS. ZHONG: Slide No. 41, please.

23 Counsel mentioned that based on the prosecution history  
24 we should be limited to construing the term to the -- the  
25 'before' term to 'during one or more previous memory



1 operations'. One thing they forgot to mention in claim 15 is  
2 not one of the ones that's actually been amended. Claim 15  
3 retained its original language--"before receiving the input  
4 command address signals corresponding to the memory read  
5 operation at the memory module control device, determining the  
6 first pre-determined amount based at least on signals received  
7 by the first data buffer." The claim is not amended.

8       Whatever we said about the other claims simply does not  
9 apply here. There is no reason, as Your Honor has pointed  
10 out, there is no ambiguity as to when the step needs to  
11 happen. The only limitation in the original claim is before  
12 the receiving step this happens. It can happen during one or  
13 more previous operations, and -- but it doesn't have to. And  
14 whether in that particular case the one or more previous  
15 operations constitutes what Samsung believes to be a memory  
16 operation is also not at issue here.

17       What Samsung really is trying to do is trying to bring in  
18 their interpretation of the memory operation into this term.  
19 That's not -- really there is no basis in either the claim  
20 language itself or the prosecution history.

21       So Your Honor has got it right. It should be construed  
22 by its plain and ordinary meaning, which is as the claim says.

23       With this we rest.

24       THE COURT: All right. Thank you, Ms. Zhong.

25       DOCTOR ALBERT: Just a very quick remark, Your

1 Honor. That claim 15 wasn't amended is of no moment. What  
2 matters here, Your Honor, is that during prosecution they  
3 told the Patent Office that these terms, this language was  
4 equivalence. Netlist can't take that back and say now it's  
5 not equivalence; now -- we meant it for the other claims as  
6 equivalent, but we don't mean it for this claim.

7 THE COURT: Why isn't their statement limited to  
8 the claims that they were talking about and the claims they  
9 were amending?

10 DOCTOR ALBERT: It just doesn't work that way, Your  
11 Honor. When you say to the Patent Office this language,  
12 wherever it is used, this language is the same, no -- the  
13 claims were amended to address minor issues of clarity, so  
14 this language that they took before, they changed it to  
15 something else to address minor issues of clarity, it means  
16 the same thing. Now, we find that same language in the claims  
17 that are -- in the claim that we're talking about here.

18 So yes, they didn't amend this specific claim, but the  
19 arguments that they made regarding the language, the common  
20 language for this claim, the claim 14 as issued, claim 15  
21 during the prosecution, would still apply; otherwise, their  
22 statement to the Patent Office wouldn't be true.

23 THE COURT: Their statement to the Patent Office was  
24 that the scope of those amended claims was -- had no new  
25 matter added. Right? I fail to see how you can just assume

1       that the same thing would have been true for any other place  
2       that language appears.

3               DOCTOR ALBERT: Fair question, Your Honor, and I  
4       appreciate the insight there. The -- if you're asking the  
5       question for these claims why hasn't there been new matter  
6       added, for all these other claims that were amended why has  
7       there not been new matter added if you change the language,  
8       the only way that could be true is if those -- that new  
9       language didn't increase the scope, didn't change the scope  
10      of that claim so, therefore, that language was equivalence.

11             THE COURT: Okay.

12             DOCTOR ALBERT: And so for claim 15, we find that  
13      same language in there. Yes, they didn't make the argument  
14      regarding claim 15--very good insight, Your Honor, we  
15      appreciate that--but they did make the argument with regards  
16      to the language that is found in claim 15, as issued claim 14.

17             THE COURT: Except that it's not the same language.

18             DOCTOR ALBERT: It includes broader language, but it  
19      includes the same -- references the same memory read  
20      operation.

21             THE COURT: You have a tough argument, but you've  
22      made it well. Thank you.

23             DOCTOR ALBERT: Thank you, Your Honor. I appreciate  
24      the attention.

25             THE COURT: Sure.

1 DOCTOR ALBERT: So we'll move on now to the drive  
2 terms.

3 THE COURT: All right.

4 DOCTOR ALBERT: The core dispute with regards to  
5 these drive terms is whether the buffer as described in the  
6 '339 Patent requires switching between different data pass.  
7 Sometimes that's colloquially referred to as a fork in the  
8 road where the buffer is -- has outputs to different memory  
9 devices and it could switch between groups of memory devices,  
10 kind of like a fork in the road.

11 And so here we have in the proposed construction the idea  
12 is expressed by activating certain groups of memory devices  
13 while at the same time deactivating other devices. You select  
14 between one group and another group. And we're talking about  
15 a number of claims here, but they all have this drive concept,  
16 it's built into this very large claim -- you know, very large  
17 limitation. I apologize for that, Your Honor. We didn't  
18 write the claim; we just have to try to figure out what it  
19 means. But here we have this idea that you have this logic  
20 configurable to control the data path seen in claim 1. It  
21 actively drives the section of the data from a first side to  
22 a second side. So the question is, for this patent with this  
23 prosecution, what does that -- what do those drive terms mean?  
24 Does it include that fork in the road?

25 If you look to the '339 Patent, these data buffers are

1 really to accomplish two things, and the first is "to  
2 electrically couple only the enabled memory devices to the  
3 memory controller"--and so here I've got this highlighted in  
4 yellow on the left--"by using the data transmission  
5 circuits"--that's also called the buffer--"to electrically  
6 couple only the enabled memory devices to the memory  
7 controller." Now why is it doing that? It says it right  
8 there at the top--"to reduce the memory device loads seen by  
9 the system memory controller."

10 So their idea was that memory -- that loads were a  
11 problem, and to address that problem, they would isolate and  
12 couple -- isolate some groups of memory devices; couple other  
13 groups.

14 So you move onto the second function is "to electrically  
15 isolate the other memory devices which are not performing the  
16 memory operation"--and here I've got it highlighted in pink on  
17 the lower left--"and to isolate"--excuse me--"electrically  
18 isolate the other memory devices 412 from the memory  
19 controller." So this idea --

20 THE COURT: All of that is described as 'desirably  
21 achieved in certain embodiments'. Right?

22 DOCTOR ALBERT: Well, there are no other  
23 embodiments, Your Honor. And there is a dispute about that,  
24 and I will go through that.

25 THE COURT: Okay.

1 DOCTOR ALBERT: The reason, the basis, the  
2 motivation behind this coupling and isolation and switching  
3 between the two paths is to reduce the device loads. And as  
4 Your Honor is well aware that this problem to be solved is an  
5 important consideration in claim construction.

6 So here I have an illustration of figure 5, and I'll walk  
7 through that. That shows exactly how this is described in the  
8 patents--excuse me--in the '339 Patent. And the core concept  
9 from figure 5 is this path A and path B. Here I've got that  
10 highlighted in figure 5. The text is, "Whereby the control  
11 logic circuitry selects either path A or path B to direct the  
12 data." So you can send the data one way or you can send the  
13 data a different way. You're selecting between the paths.  
14 The selection that the patent is talking about is the  
15 selection between two different paths. And going back again,  
16 that selection is to address the problem of the device memory  
17 loads.

18 So going back to figure 5, it goes on, "When the control  
19 logic circuitry receives, for example, an enable A signal."  
20 So I've got this enable A signal that turns on this top A  
21 path. The top A path has a tristate buffer. It's labeled  
22 504. That's enabled and actively drives the data value on its  
23 output, while the second tristate buffer 506--so I have marked  
24 out in red--is disabled with its in output a high impedance  
25 condition. So you have a selection between a path A and a

1 path B.

2 So here we just have that illustration. In this state  
3 the data transmission circuit allow it is data here from --  
4 you know, from the 420 line to go up through the tristate  
5 buffer and onto Y1, which is that path A.

6 Here is just another figure showing the same idea. Here  
7 we have a -- the buffers are transmission circuits 416 kind of  
8 in the left middle just to the left of the highlighting, and  
9 they in path A are connected to two sets of memory devices.  
10 They're not connected to all memory devices; they're connected  
11 to two sets. So you've got this path A that connects to this  
12 we'll call ranks A and C.

13 Now, the patent also talks about the alternative if you  
14 want to go down path B. So if you enable B, then what you're  
15 going to have there is that the tristate buffer A that was  
16 previously activated and turned on, that is closed. Path B  
17 becomes open; path A becomes closed. And now here the data is  
18 directed to that path B terminal Y2. And that, again, is  
19 illustrated in a different figure in figure 3A. Instead of  
20 the A and C ranks being activated, the B and D ranks are  
21 activated.

22 So you've got this idea between a path A and a path B  
23 where some memory devices are accessed in path A and some are  
24 accessed in path B. Again, it's to implement this idea that  
25 they have this problem they are trying to solve of reducing

1 the load. This was their solution to the problem that the  
2 named inventors perceived.

3 There's a similar description on the receive side. If  
4 you -- receiving data from the memory elements into that Y1  
5 and Y2 terminals, then the patent has a way to deal with that,  
6 and that is this multiplexer 508--I've got that  
7 highlighted--and what the patent does is it says, Well, I've  
8 got this two different inputs; I'm going to select -- selects  
9 one route to it's output. So again, we have two paths, the  
10 selection -- this concept of selection between two different  
11 paths.

12 And going through the patent, time and time again the  
13 patent is talking about the selection selectively allowing or  
14 inhibiting the data paths. Here we have some examples. '339  
15 8, 41 through 53 references the module control signals by  
16 selecting or allowing the data transmission between the system  
17 memory controller, column 339--excuse me--column 10, 64  
18 through 11:4 it's discussing these load reducing switching  
19 circuits. So again, we see that switching language to  
20 describe reducing the load by switching the paths between a  
21 path A or path B or group A and group B with this idea of this  
22 selectively switching between the paths is referenced over and  
23 over again in the patents.

24 Here we got it again at 11:35 to 44 discussing "data  
25 transmission circuit selectively switches between two or more



1 memory devices." 15:33 through 38, it switches a single data  
2 line between the memory controller and the memory device.  
3 Again, switching, switching, switching. It is talking about  
4 that concept over and over again. '339, 17:30 to 44 talks  
5 about enabling the proper data pass between the system memory  
6 controller and the targeted or selected memory devices.

7 That right there is enough, Your Honor. The consistent  
8 and uniform description of the patent with the idea of the  
9 switching illustrates the concept of the -- what these claims  
10 are meant to cover; what these claims do cover by enabling the  
11 data paths, according to the claim language; by driving the  
12 signal from one side to the other, according to the claim  
13 language.

14 But the patentee also distinguished prior art during  
15 prosecution. One of the pieces of prior art was this prior  
16 art Ellsberry, and it says, "Ellsberry does not  
17 disclose"--this is what Netlist said during  
18 prosecution--"disabling data paths in its memory bank  
19 switches. The claimed invention allows controlling of the  
20 data paths between the memory devices and the bus interface."  
21 They go on to say, "On the contrary, Ellsberry teaches away  
22 from switching the data paths in its memory banks." Again,  
23 very -- you know, this same language is repeated over and over  
24 again in the specification--switching the data paths.

25 So we have, again, going back to that claim language of

1 driving the different data paths and selecting and switching  
2 between those data paths again all comes back to reducing --  
3 this is this solution for -- that the patentee chose to  
4 implement their -- the solution to the perceived problem of  
5 load on the system.

6 Now, there is a dispute about whether the specification  
7 actually does disclose an alternative embodiment, whether  
8 there is a reference to an embodiment where there isn't a  
9 switching between data paths. And Netlist makes a -- puts  
10 this in the brief. This is -- I have the language that  
11 Netlist put in their brief, and the bolded and italicized  
12 section is the same language that Netlist bolded and  
13 italicized in their brief, I believe. What they didn't do,  
14 however, is point Your Honor to the highlighted portions which  
15 I'd like to discuss.

16 So this language, "One or more of the data transmission  
17 circuits 416 in accordance with an embodiment of the  
18 disclosure is operatively coupled to one or more of the data  
19 lines 452 connected to one or more memory devices in each of  
20 the ranks." Now, Netlist makes a big deal about the  
21 recitation of the one saying, Well, that's the idea, there is  
22 no fork; that there can be no fork if there's only one, but  
23 that's not what -- where this sentence ends, because this  
24 sentence ends with "in each of the ranks A, B, C, D." And if  
25 I have a data line to a device, memory device, but for each

1 rank that's going to be multiple data lines, that's going to  
2 be multiple paths.

3 And it repeats it again down below, but then it  
4 specifically references figure 3 as an illustration of this  
5 concept. And Your Honor, we already saw figure 3. I showed  
6 it to you just a few minutes ago, but here is figure 3 again  
7 where I've repeated the highlighting from my earlier slides  
8 where we don't see in figure 3 a single line, a single  
9 straight line embodiment, as Netlist has coined the phrase,  
10 but a -- again, a fork-in-the-road embodiment where it goes to  
11 one group for one path and another group for another path. So  
12 this language that Netlist places so much stock into is really  
13 just an illustration again of figure 3A which shows the fork  
14 in the road.

15 So what does Netlist then do? Netlist then takes this  
16 concept, this single word out of context and says, Well, if it  
17 does mean one, then we can just change all of the figures to  
18 have a straight line embodiment. And this was kind of strange  
19 to us because I've never seen this in a brief, but they've  
20 taken figures and erased portions of the figures to say,  
21 *Voila*, there is your straight line embodiment; there is your  
22 no fork in the road? But what they've done is they've erased  
23 and deleted parts of the figure that describe the fork in the  
24 road. So they did it here for figure 4, they did it for  
25 figure 3, they blacked out this -- the other prong of the fork

1 to claim that there is now a -- not a fork in the road here.  
2 But the figures themselves describe this fork-in-the-road  
3 concept; the patent specifically describes this  
4 fork-in-the-road concept. And it's very uniform in that  
5 description about that switching between the data paths.

6 This was in their reply brief, a reference to 16:38  
7 through 45. "In yet another embodiment, the multiplexer and  
8 the read buffer operations may be split over two tristate  
9 buffers, one to enable the value of Y1 and another to enable  
10 the value from Y2." And sometimes they claim the tristate  
11 buffers can operate independently and, therefore, that somehow  
12 shows the straight line embodiments.

13 And so what I have here on the right--I'll be very  
14 clear--this was our attempt to try to put into a picture what  
15 was described, but we didn't see a picture in the brief so  
16 this is our attempt to replace the multiplexer with these two  
17 red tristate buffers. So what I have here in red is not in  
18 the patent; it's an attempt to illustrate the replacement of  
19 the multiplexer that's described in the specification as  
20 another possibility.

21 And Netlist says, Well, if those two tristate buffers  
22 operate independently, then that would be a straight line  
23 embodiment because you'd have independent operation. And  
24 there's two things that are wrong with that that we saw in  
25 their reply brief is that, one, we -- the patent doesn't

1 describe 'independent operation' of these replacement tristate  
2 buffers; it just mentions that you can do it in -- you know,  
3 in some way. It doesn't describe 'independent operation'. Go  
4 through the patent; it's going to be nothing that describes  
5 that.

6 And you wouldn't do it that way because that wouldn't  
7 work. If you had these two tristate buffers and you were  
8 operating them independently, both of them are receiving  
9 memory read operations--or sorry--data from the memory devices  
10 through this Y1 and Y2, if they are single lines, you know,  
11 single straight line embodiments, what's going to happen is  
12 that that independent operation--again, not in the  
13 patent--would cause that data to merge onto the same line and  
14 crash together. That's not a product or an idea that you'd  
15 want to implement.

16 So the patent doesn't describe this independent  
17 operation. Netlist says that you could do it independently,  
18 but that's not described in the patent. So again, this is  
19 another thing that Netlist pointed to as somehow describing an  
20 alternative embodiment that it could be a straight line  
21 configuration or not a fork in the road, but the point here is  
22 it doesn't disclose that, and the way Netlist argues they  
23 would work would cause the system problems.

24 Netlist put a lot of stock into two prior ITC cases, the  
25 1023 investigation, 1089 investigation, arguing that, Well,

1 for the 1023 investigation that that involved different claim  
2 language and that claim language isn't involved here; so even  
3 though the 1023 found that those claims required a  
4 fork-in-the-road implementation, that same exact claim  
5 language is not found in this case. The claim language that  
6 was issued there was this 'selectively isolate selectively  
7 allow' language. But again, that's the same language,  
8 'selectively', that was repeated over and over in the  
9 specification but also in the prosecution in -- for this  
10 patent.

11 And then for the 1089 investigation, the -- that was a  
12 bit of a strange posture, Your Honor, because the ALJ decides  
13 an issue and then the commission gets to review it. And here  
14 the ALJ reviewed the fork issue, found for those claims didn't  
15 require a fork, but the commission reversed the infringement  
16 finding, and it did that on this term 'receive' which required  
17 that all of the--excuse me--that -- and built into this  
18 'receive' concept was this idea that not all of the memory  
19 elements could receive the memory operations. In other words,  
20 some would receive it, some would not, and because the  
21 products in that case, all of them received the memory  
22 operations, there is no infringement.

23 So again, we have the split between some devices having  
24 some access, access -- memory operations grouped between a  
25 different set of devices. And so, again, the commission

1 didn't use the word 'fork in the road' to specifically  
2 implement its decision, but built into that concept, built  
3 into that decision and that concept was this fork-in-the-road  
4 idea.

5 But again, we're not relying -- we're not saying that  
6 these two cases are controlling. We're asking the Court to  
7 look at the facts of this case, the claim language of this  
8 case where the claim language discusses the driving of the  
9 data, activating the pass, and the prosecution history of this  
10 case which describes the selection that was used to circumvent  
11 the prior art.

12 THE COURT: Mr. Albert, can you go back to your  
13 slide with figure 5 from the patent; not the modified version,  
14 but the actual version?

15 The fork in the road that you're describing is the place  
16 where path A and path B split off at the top of figure 5  
17 there. Is that right?

18 DOCTOR ALBERT: That's exactly right, Your Honor.  
19 So we'd have the two paths, path A and path B going -- and  
20 they would go through different terminals, Y1 and Y2.

21 THE COURT: Do you contend that you cannot drive a  
22 signal along path A without disabling path B? In other words,  
23 are you taking the position that it's not electrically  
24 possible to do that?

25 DOCTOR ALBERT: Well, that's -- the patent doesn't

1 describe a dual operation of both path A and path B.

2 THE COURT: I know. My question is a different  
3 question. Do you contend that you cannot drive a signal along  
4 path A without disabling path B?

5 DOCTOR ALBERT: Not with this circuit as disclosed  
6 in the '339. Now --

7 THE COURT: I don't know what that means.

8 DOCTOR ALBERT: Engineers are very bright, and you  
9 can certainly create a different circuit with a different  
10 disclosure that could drive different pins at the same time,  
11 but that's not the disclosure or the circuit we are discussing  
12 here. The disclosure for this circuit would be in either path  
13 A or path B.

14 THE COURT: All right. And my question is do you  
15 contend that you cannot drive a signal along path A of this  
16 circuit without disabling path B.

17 DOCTOR ALBERT: Yes, that is the way that the patent  
18 describes the path A path B operation.

19 THE COURT: All right. So you're answering about  
20 your interpretation of the disclosure in the specification and  
21 I'm asking about the figure as it appears there, but  
22 anyway --

23 DOCTOR ALBERT: To put a finer point on that, Your  
24 Honor--I don't mean to duck your question--the -- if you look  
25 to see, there is a control going into the tristate buffers



1     that we have -- you know, 430 goes into 502, and then that  
2     controls the different tristate buffers. The way that this  
3     circuit operates, the way that this circuit -- this particular  
4     circuit with this control scheme operates is that you would  
5     not be able to drive it onto path A and path B because of that  
6     control circuit. Now, if we took out parts of the figure  
7     where there wasn't that control and put something else in,  
8     then, you know, maybe it might be possible, but I'm -- we're  
9     not seeing it with this control circuit.

10           THE COURT: All right. Mr. Albert, let me go ahead  
11     and take the morning recess now. We'll come back and hear if  
12     you have additional remarks and then the response.

13           DOCTOR ALBERT: Thank you, Your Honor.

14           THE COURT: Thank you.

15                     (Brief recess.)

16           THE COURT: Thank you. Please be seated.

17           Mr. Albert, do you have anything further on this term?

18           DOCTOR ALBERT: Nothing further on this term, Your  
19     Honor.

20           THE COURT: All right. Thank you, sir.

21           MS. ZHONG: So the counsel has argued at length  
22     focusing on the full rank embodiment of the '339 Patent. What  
23     the counsel fails to mention is that the specification is very  
24     clear. Even though the description is with respect to four  
25     ranks, embodiments with less than four ranks, including two

1 ranks per memory record 402, 402 prime may be employed. And  
2 why is that important? It is important because if you only  
3 have two ranks, a single path is sufficient.

4 For example, if we look at figures 3A, there are two 452  
5 lines--one 452 connecting the purple colored 416, which is a  
6 data buffer, to ranks A and C. There is a second one that we  
7 have grayed out that's connecting data buffer 416 to the two  
8 other ranks B and D. But if you only have two ranks, A and C,  
9 a single pass is needed, so there is no need for the fork in  
10 the road. That's a straight line configuration there. And if  
11 we don't have a second line, disabling the second line just  
12 doesn't make any sense. And the claim does not require that  
13 there be four ranks with two different paths.

14 And why do we know that the two ranks is actually  
15 contemplated by the invention? Let's go back to what the  
16 counsel said. The purpose of this invention is load  
17 reduction. If Your Honor take a look at figure 2A, figure 2A  
18 as described in columns 5, lines 44 to 64, that's a prior art  
19 configuration with two ranks. And in particular, in column 5,  
20 lines 45 to 48, the inventors described that with respect to  
21 the two-rank operation there is a load problem. Sorry. I got  
22 the lines wrong. The lines that's relevant to the load  
23 reduction starts actually column 5, lines 59.

24 So with respect to two-rank, they say, "Therefore, during  
25 a write operation, the system memory controller 220 sees all

1 the memory devices 212 as its load, the other data lines 250."  
2 That is, it sees two ranks of memory modules.

3 And what does our invention do? Regardless of the number  
4 of ranks, the invention allows you to -- the memory controller  
5 to see a single rank. Where is that disclosed? That's  
6 disclosed, for example, in column 14, starting at line 59. It  
7 says, "To reduce a memory device load seen by the system  
8 memory controller 420, e.g., during a write operation, the  
9 data transmission circuit 416 of certain embodiment is  
10 configured to be recognized by the system memory controller  
11 420 as a single memory load."

12 So even for two-rank, it used to be in a prior art, the  
13 memory module sees two ranks of memories and now it sees as a  
14 single load, a single rank. So there is load reduction there  
15 for two-rank. And for the two-rank, as I show on screen here,  
16 a single line is sufficient. You don't need to have a second  
17 -- what they call the fork in the road. Without the fork in  
18 the road, disabling the second path, as they suggest, is just  
19 not justified.

20 Now, I understood that counsel said during prosecution we  
21 were talking about selecting or switching the pass on and off.  
22 I think it's a misunderstanding of what we were actually  
23 saying.

24 So let's look at column -- slide No. 10.

25 The argument is actually saying the data passing

1 Ellsberry switches 206/208 are opened by default. What our  
2 claim is really requiring is that that particular path is  
3 turned on during a specific time period, and when the data  
4 passes on the operation -- the write data or read data is  
5 passed on the data pass are then turned off. So when the  
6 counsel is talking about switching on, selecting on and off,  
7 they're not talking about switching between different paths;  
8 they're talking about a single path A is switched on during  
9 specific time period. So they're talking about temporal  
10 turning on and off, not physical, spatial turning on from --  
11 switching from one pass to another. So that was a complete  
12 misrepresentation of what we argued during prosecution.

13 With respect to Your Honor's question regarding figure  
14 No. 5 --

15 Maybe slide No. 18, please.

16 Figure No. 5, Your Honor asked whether in this particular  
17 embodiment it has to be the case that the second pass is  
18 turned off. Our understanding is that it doesn't have to be.  
19 It can be turned on as in prior art. You can use, for  
20 example, a technique called data masking for the write path  
21 and the data can be sent and only be selected -- only received  
22 -- the useful data is only received by the memory device  
23 that's intended to receive the data where the write -- so the  
24 data pass can be open, like both can be on at the same time.

25 THE COURT: Would that serve the goals of the

1 invention in this patent?

2 MS. ZHONG: So if you do that, I think you do see  
3 some load reduction, not as much, so instead of, like,  
4 reducing the load from four loads to one load, you may be  
5 reducing it from four loads to two loads.

6 THE COURT: All right.

7 MS. ZHONG: Okay. Does Your Honor have additional  
8 questions? If not, we will rest.

9 THE COURT: I think I understand your position on  
10 it. Thank you.

11 Mr. Albert, if you want to respond, you may.

12 DOCTOR ALBERT: Thank you, Your Honor.

13 Just a couple of points here.

14 With regards to the point about the possibility of a  
15 two-rank system and the argument that, Well, the patent in  
16 this invention could have been implemented not using this fork  
17 in the road with two ranks, I kept hearing 'could have',  
18 'didn't have to be', 'could have been implemented'. That's  
19 not what the specification says. When the specification  
20 implements this invention, it is always with that fork in the  
21 road. And in order to be able to concoct a straight line  
22 embodiment without a fork in the road, Netlist has had to  
23 alter the figures in the patent, which is telling.

24 So this idea that you could have done something  
25 differently, that -- Your Honor, that is the case with every

1 single patent that falls in front of you--that you could have  
2 done things differently. The question before this Court is  
3 what was disclosed in this specification and this prosecution  
4 history. And this prosecution history, again, Netlist in its  
5 briefing, you know, put big emphasis on that 'switching'  
6 language in the ITC case, and that same language is found in  
7 the prosecution history--switching of the data lines.

8 So with that, unless Your Honor has any further  
9 questions.

10 THE COURT: You know, Mr. Albert, one of the  
11 problems that this proposed construction faces is the fact  
12 that you're construing one word with what is probably 200  
13 words. I am -- I don't know that I've ever seen a more  
14 elaborate proposed construction for a single term.

15 DOCTOR ALBERT: And I'm glad Your Honor asked that  
16 question because, unfortunately, this is a byproduct of  
17 repeated litigation by Netlist. Netlist asserted these  
18 patents in this family against similar technology, was found  
19 not to infringe, got continuations repeated, and there's been  
20 this serial continuing prosecution for these patents to make  
21 longer and longer claims, more complicated claims for this  
22 simple idea that there is a fork in the road.

23 So what we have here is not just the word 'drive' that's  
24 being construed, Your Honor, because it's not just 'drive' in  
25 the abstract; it's 'drive' -- let me just take claim 1, for

1 example. This whole phrase, this complicated phrase that  
2 Netlist has put in their patent all goes to this concept of  
3 the fork in the road of this switching. It starts with the  
4 buffer, including the logic configurable to control the data  
5 path. Again, we saw in the specification that that path A  
6 control and that path B control, splitting the two paths, the  
7 path that the data would ultimately follow and switching  
8 between the one group of memory versus the other group of  
9 memory, that's built into this phrase as well as other  
10 portions of this claim.

11 It goes on to say that the data path is enabled.  
12 Enabled. So we're enabling and disabling data paths. So  
13 we're -- we have that logic to control the data path, just  
14 like that path A and path B embodiment that we saw in the spec  
15 that was repeated over and over and over again, the only way  
16 that the control is described.

17 And then it talks about driving the data from one side of  
18 the buffer to the other side of the buffer. And again, the  
19 only way the patent describes that driving, that -- from one  
20 side to the other is with this fork in the road. You drive it  
21 from, you know, one group or the other group.

22 And then it talks about the -- again, the tristate  
23 buffers. I showed those to you in figure 5 where you enable  
24 path A, you are enabling the path A tristate buffer and  
25 correspondingly disabling because of that control circuitry

1 the path B.

2 So it's not just a single word that's been construed,  
3 Your Honor; it's the entire collection of this language. Very  
4 complicated, we understand, but it's really results of this  
5 continuing serial application that Netlist has undergone.

6 THE COURT: All right. Thank you, Mr. Albert.

7 DOCTOR ALBERT: With that, we will rest on the  
8 papers for 'module controller', the next term, Your Honor.

9 THE COURT: All right.

10 MR. SHEASBY: Your Honor, Mr. Tezyan was going to  
11 argue that term, and I would like to represent to the Court  
12 that he was awesome when we went through it yesterday and it  
13 would have been his first argument. So if we could get  
14 judicial notice of that, I would appreciate it.

15 THE COURT: All right. We'll direct that his  
16 remarks be placed in the record.

17 MR. SHEASBY: Can I have the elmo, Madam Courtroom  
18 Deputy?

19 So this is the last term that we are arguing, and the  
20 attention is -- and I appreciate the Court's indulgence by not  
21 just saying 'plain and ordinary meaning', but actually wading  
22 into the dispute. And I think everyone agrees, if you go back  
23 and look at the specification, the portion of the  
24 specification that guides this is column 50, lines 60, *et seq*,  
25 to column 16, lines 5. And the only point I will make, Your



1 Honor, is in that section I have highlighted the relevant time  
2 period. The latency is not just the moment that it starts;  
3 it's also the moment that it stops as well.

4 In the construction as given in a time period where the  
5 start of -- wherein the start of the time period depends on at  
6 least the latency parameter, it would create significant  
7 difficulty in applying the claim during the infringement phase  
8 of the case if the back end of the latency period was not  
9 defined.

10 And so consistent with column 15, we would ask that the  
11 language -- in fact, we'd be comfortable with the language  
12 directly from there where it says "from the moment the memory  
13 controller starts to it stops". If we could just use that  
14 exact language, we would appreciate it, because it is going to  
15 create confusion at the time period in the subsequent case.  
16 And I think that a period of time has a beginning and an end.  
17 I don't think that's in dispute. And the latency controls  
18 both the beginning and the end of that time period, and we'd  
19 like to make that clear based on the specification that I just  
20 read, Your Honor.

21 THE COURT: All right.

22 DOCTOR ALBERT: Admittedly, Your Honor, I don't know  
23 what to make of that. I don't know what's being proposed by  
24 Netlist at this point, and I don't know what the dispute is  
25 given the statements.

1 THE COURT: It's my understanding of their statement  
2 that they are still seeking duration, but that they feel they  
3 can get there if the construction includes both the start and  
4 the end.

5 DOCTOR ALBERT: And here, Your Honor, perhaps a  
6 little bit of clarity as to our understanding would be helpful  
7 here.

8 So if you look at the claim language, 'time period in  
9 accordance with a latency parameter', Your Honor's  
10 construction follows that 'a time period wherein the start of  
11 the time period depends on at least a latency parameter'.  
12 That was different than Netlist had sought, which is the start  
13 and duration depending on a latency parameter. So my  
14 understanding of the tentative was that the 'and the  
15 duration' was excluded from the construction.

16 THE COURT: That was a correct understanding.

17 DOCTOR ALBERT: And so as Your Honor distinctly  
18 tuned into here, the specification discusses latency  
19 parameter, discusses latency, and talks about latency is a  
20 delay time--right?--something that elapses between one event  
21 and another. And Netlist's original construction -- I don't  
22 quite know if that's what their getting at right now, but  
23 their original construction was not just a delay time--which,  
24 you know, you could also call that a duration, a duration of a  
25 delay--they wanted a construction of a latency parameter to

1 include the duration of delay--you know, that delay time--but  
2 also a second duration, and that's where we have issue with.

3 So we -- Your Honor correctly and keenly tuned into the  
4 real issue here that latency is that delay time, as is  
5 described in the specification, and the -- it requires no  
6 further construction than that. The patent itself says that  
7 this is a known thing in the field. Patent -- I couldn't tell  
8 whether counsel was saying that the specific description in  
9 the patent was an expressed definition that changed the  
10 meaning in the field, that differed from the meaning in the  
11 field, but the patent acknowledges that this is a known  
12 parameter and then goes on to describe it as a delay, and just  
13 like Your Honor's construction of a time period where the  
14 start of the period depends at least on a latency parameter.

15 THE COURT: I think what we're really construing is  
16 what 'time period in accordance with' means here, because I  
17 agree with you that there seems to be agreement about what the  
18 latency parameter itself is.

19 DOCTOR ALBERT: And the original dispute that -- as  
20 I understood it from the briefing, Your Honor, was Netlist  
21 seemed to be trying to redefine the term 'in accordance with',  
22 which didn't argue in the brief that 'in accordance with' had  
23 a very specific meaning, but that was the implication of their  
24 argument.

25 You know, based on the Court's construction, you know, we

1 don't have any further points here.

2 I would just go on to say, Your Honor, that, you know,  
3 there is an IPR outstanding on this issue, as Your Honor may  
4 know. After the briefing finished, the institution decision  
5 came out instituting on all claims. And the Patent Office  
6 sided with Samsung's construction here, which would be  
7 consistent with Your Honor's construction that it -- the  
8 time period of that starts based on the latency parameter.

9 So with that and, you know, barring further clarification  
10 from Netlist counsel as to whether they mean something other  
11 than what Your Honor has written down, we have no further  
12 points here.

13 THE COURT: All right. Thank you, Mr. Albert.

14 MR. SHEASBY: Your Honor, I wrote down what counsel  
15 said is he, quote, elapses between one time and another as the  
16 period, and we agree with that. What we're trying to make  
17 clear, and we understand that our proposed construction had  
18 issues with sort of second latency period or things like that,  
19 that was not our intention. Our point is that the latency  
20 period is between two moments. It's not just -- it doesn't  
21 just control when the period -- the latency parameter doesn't  
22 just control when the period starts; it also controls where  
23 the period ends, of necessity. And I think if 15, line 61  
24 through 65, which is the same passage that they quote in their  
25 brief--they just allied part of that--makes it clear that the

1 period from when it starts to when it ends, and that's the  
2 only request we would make consistent with the specification,  
3 Your Honor.

4 THE COURT: Well, if the latency parameter is clear,  
5 why doesn't 'using it to set the start time' resolve the whole  
6 thing?

7 MR. SHEASBY: Because it -- using it -- they will  
8 take the position that 'using a latency parameter to set the  
9 start time doesn't mean that the latency parameter controls  
10 the end time. So they -- their position technically will be  
11 that they're not necessarily linked, they're not inherently  
12 linked; you can start one -- you can have it start it but not  
13 have it when it ends.

14 And so our position is in the specification to latency  
15 period, in column 15, lines 61 through 65 makes clear that the  
16 latency period is not just the beginning, it's the end. And  
17 I'll read that into the record. "The column addressed strobe  
18 latency"--that's what we're referring to here; I think both  
19 parties agree on that--"is the delay time which elapses  
20 between the moment the memory controller informs the memory  
21 module to access a particular column in a selected rank or row  
22 and the moment the data from the particular column is on the  
23 output pins of the selected rank or row."

24 And so the latency parameter controls the entire  
25 period--not just when it starts, but when it ends. And

1 Samsung will take the position that it's not inherent, that  
2 when it starts -- controlling when it starts means you're  
3 controlling when it ends.

4 THE COURT: All right.

5 MR. SHEASBY: Thank you, Your Honor.

6 THE COURT: Thank you.

7 DOCTOR ALBERT: Your Honor, as I understand,  
8 Netlist's position is just a rephrasing of their prior  
9 construction a time period with the start of the time period  
10 and the duration of the time period depends on at least the  
11 latency parameter.

12 THE COURT: Mr. Albert, can you describe your  
13 position through the use of figure 6? I saw that you had a  
14 slide on that a little earlier.

15 DOCTOR ALBERT: Yes. So figure 6 is instructive,  
16 Your Honor, because there are -- the patent describes  
17 'latency', and with regards to figure 6, the patent also  
18 describes these time periods 601, 602, 603. The patent uses  
19 different language for that -- to describe latency and the  
20 periods. It doesn't link the two together like Netlist's  
21 construction is now linking.

22 Latency is just a delay of time. It's found in their  
23 own dictionary definition they cited. It's a delay time.  
24 We agree it's a delay time. But that's not the crux of the  
25 issue, because the crux of the issue is that the -- as Your

1 Honor pointed out with Netlist's -- the dispute really seems  
2 to be now is the language period 'in accordance with', and  
3 what does that mean; how narrow is that term. And Your Honor  
4 correctly pointed out that 'in accordance' means it could be  
5 dependent on the start time.

6 Now, does 'in accordance' mean, as Netlist seems to now  
7 imply, that every variable has to be defined for that period  
8 for 'in accordance'? No. That's not what 'in accordance'  
9 means. And if you actually look at the patent, 'in accordance  
10 with' is used throughout the patent to describe various  
11 things, including some of the figures, which don't have all of  
12 the description from the specification. 'In accordance with'  
13 is -- in the patent is used as a general term. It could be  
14 used as 'depend on', just like Your Honor has found.

15 So with that, with the evidence in the record, we believe  
16 Your Honor has gotten this one correct.

17 THE COURT: The claim language in claim 1 that talks  
18 about the latency parameter refers to the path -- data path  
19 being enabled for a first time period in accordance with the  
20 latency parameter. So is your understanding of the plain  
21 meaning of that that the latency parameter determines when it  
22 starts, but the claim does not dictate when that enablement of  
23 the path ends?

24 DOCTOR ALBERT: Yes, Your Honor, that would be  
25 sufficient. And that's -- again, that's exactly what the

1 Patent Office just found in its institution decision regarding  
2 these claims.

3 THE COURT: All right.

4 DOCTOR ALBERT: And I can put that language up, Your  
5 Honor. "On this record we are sufficiently persuaded by  
6 Petitioner's argument that enabling the data path for a time  
7 period that starts based on the latency parameter. The patent  
8 owner does not sufficiently address whether claim language  
9 require latency to relate to the duration of the time periods  
10 during which the data is driven rather than the start of the  
11 time period."

12 THE COURT: Thank you.

13 MR. SHEASBY: And I'll just make the point that the  
14 duration thing is obviously -- the use of the word  
15 'duration' is obviously inartful, but I think if you look at  
16 the claim language, the latency parameter is controlling the  
17 first time period and that first time period is the beginning  
18 -- includes the beginning and end of the period.

19 So I think from the claim language itself, it's required  
20 that the latency parameter control both the first and -- the  
21 beginning and the end. And I'll read that into the record.  
22 "A latency parameter to actively drive the respective  
23 byte-wise section of the end bit wide write data associated  
24 with the memory operation from the first side to the second  
25 side during the first time period." From the first side to



1 the second side, from the beginning, the moment of the  
2 beginning to the moment at the end, Your Honor. Thank you.

3 THE COURT: And is it your understanding of latency,  
4 as used here, that it's talking about something that's  
5 inherent in the system; some number of clock cycles that is  
6 programmed in?

7 MR. SHEASBY: Yes. So it's not inherent in the  
8 system. You have to program it in. Or it's based on -- I  
9 think the tristate buffer is what actually does it, which  
10 actually delays it so that you get -- you're delaying both the  
11 start and the end so that you're not having a collision with  
12 -- in figure 6 it's depicting it in one cycle, but there's no  
13 magic to it being in just one cycle. The write process could  
14 take two cycles, for example, and when it took two cycles  
15 you'd want to make sure that the alternative tristate buffer  
16 didn't start until the end; not just that it didn't start  
17 after the beginning.

18 THE COURT: All right.

19 MR. SHEASBY: That's why it says from the moment --  
20 this is not -- that's right. This is not active. The  
21 language they put up 15:61 through 66 says it--"from the  
22 moment the memory controller informs the memory module to  
23 begin the process until the moment the process is completed."  
24 That's the whole point--the latency controls that entire  
25 period.

1 THE COURT: All right. Thank you.

2 DOCTOR ALBERT: Just one final point here.

3 It seems like Netlist is now arguing for an express  
4 definition of 'latency parameter' from the specification, but  
5 I'll point out that the language that they're pointing to is  
6 not latency parameter generally; it's a specific type of  
7 latency, column address strobe latency, which is a different  
8 term. That is a -- that's different language, different term.  
9 'Latency' can be backed out from here. It is a delay time.

10 THE COURT: So do you contend that when the claim  
11 refers to 'latency parameter', it's not referring to the  
12 'column address strobe latency' that's described in the  
13 specification?

14 DOCTOR ALBERT: This is one example of 'latency',  
15 and the examples of -- the example that has been chosen here  
16 for 'latency' is a particular type of latency--'column address  
17 strobe'.

18 Now, Netlist has offered other evidence about what  
19 'latency' means that is different that's not dependent on this  
20 'column address strobe latency', but to read this specific  
21 example of 'latency', a term that is known, into this  
22 construction, we don't believe that's proper. But the general  
23 idea of 'latency' is known. We believe that plain meaning  
24 controls. We also see that Your Honor's construction is  
25 consistent with that.

1 THE COURT: All right.

2 MR. SHEASBY: And I'll just point out for the  
3 record, this is Docket 82, page 29, it's 15:61 through 16:6,  
4 that Samsung in briefing used to describe the meaning of  
5 'latency', and that's the CAS latency passage that is up on  
6 the screen right now. So I believe there has been some drift  
7 between what was represented on papers and what was just  
8 represented now.

9 Thank you, Your Honor.

10 THE COURT: All right. Thank you.

11 Well, I take it there are no further arguments on these  
12 terms. Is that right?

13 MR. McKEON: Nothing from Samsung, Your Honor.  
14 Thank you.

15 THE COURT: All right.

16 MR. SHEASBY: Nothing from the Plaintiff, Your  
17 Honor. Thank you for your time today.

18 THE COURT: All right. The arguments have been  
19 helpful, and I will further consider them and try to get out a  
20 claim construction order promptly.

21 So with that, thank you. And we're adjourned.

22 (End of hearing.)

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I HEREBY CERTIFY THAT THE FOREGOING IS A  
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S/Shawn McRoberts 11/07/2022

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## Concordance

## &lt; Dates &gt;

**11/07/2022** 76:9.  
**NOVEMBER 4, 2022** 1:13.  
 "one 50:16.  
 '339 44:6, 44:25, 46:8, 49:4, 56:6,  
 57:22.  
 '506 36:22.  
 '918 10:18, 23:14, 23:25.  
 'before 40:3.  
 'one 39:2, 39:17, 39:18.  
 --something 66:20.  
 ...have 38:7.  
 .  
 .  
 < 1 > .  
 1 12:8, 27:19, 44:20, 62:25,  
 71:17.  
 1.8 6:19, 10:22, 11:2, 11:14, 24:2,  
 24:12, 27:4.  
 10 48:17, 59:24.  
 100 1:44, 2:48.  
 1000 2:21.  
 1023 53:25, 54:1, 54:3.  
 104 2:14.  
 1080 14:24, 15:7, 19:9.  
 1089 53:25, 54:11.  
 110 24:8.  
 1102 10:23.  
 1110 9:19.  
 1112 9:19.  
 1122 11:14.  
 1122--is 24:12.  
 11:35 48:24.  
 11:4 48:18.  
 12 14:21, 14:22, 14:24, 14:25,  
 15:3, 15:5, 15:7, 15:8, 15:11,  
 15:15, 18:25, 19:1, 19:20,  
 20:5.  
 12860 2:28.  
 13 18:25.  
 14 18:25, 42:20, 43:16, 59:6.  
 15 24:25, 41:1, 41:2, 42:1, 42:20,  
 43:12, 43:16, 65:10, 68:23,  
 69:15.  
 15--very 43:14.  
 15:33 49:1.  
 15:61 73:21, 75:3.  
 16 5:13, 5:20, 11:7, 15:1, 15:12,  
 15:16, 15:17, 16:15, 17:10,  
 18:14, 18:15, 18:21, 18:22,

19:23, 19:25, 20:1, 20:2, 20:5,  
 23:2, 64:25.  
 16:38 52:6.  
 16:6 75:3.  
 1717 2:36.  
 17:30 49:4.  
 18 10:18, 23:25, 36:7, 60:15.  
 1800 2:5.  
 1810 36:8.  
 1820 36:8.  
 1820--receiving 36:10.  
 1830 36:12.  
 1860 36:14.  
 1870 36:15.  
 1880 36:16.  
 19 36:22.  
 .  
 .  
 < 2 > .  
 2 1:5, 3:3, 37:18, 38:1.  
 2.5 6:5, 12:8.  
 200 62:12.  
 20024 2:22.  
 202 2:23.  
 203-7096 2:8.  
 206/208 60:1.  
 206A 33:25.  
 21-CV-463-JRG 1:5.  
 212 59:1.  
 214 2:38.  
 220 58:25.  
 221-463 3:3.  
 23 23:13.  
 250 59:1.  
 26 19:7, 19:8, 19:19.  
 29 5:20, 6:5, 6:25, 10:18, 23:14,  
 23:25, 27:2, 75:3.  
 2A 58:17.  
 .  
 .  
 < 3 > .  
 3 38:1, 51:4, 51:5, 51:6, 51:8,  
 51:25.  
 30 19:21, 24:25.  
 300 2:14.  
 303 2:42.  
 310 2:8.  
 33 6:25, 27:2.  
 339 48:14.  
 339--excuse 48:17.

35 19:7, 19:8.  
 38 49:1.  
 39 18:21.  
 3A 47:19, 51:13, 58:4.  
 .  
 .  
 < 4 > .  
 4 36:22, 38:1, 51:24.  
 400 2:28.  
 402 58:1.  
 41 18:22, 40:22, 48:15.  
 412 45:18.  
 416 47:7, 50:17, 58:5, 58:7,  
 59:9.  
 420 47:4, 59:8, 59:11.  
 430 57:1.  
 44 48:24, 49:4, 58:18.  
 45 52:7, 58:20.  
 452 50:19, 58:4, 58:5.  
 46 5:21.  
 48 58:20.  
 .  
 .  
 < 5 > .  
 5 38:1, 46:6, 46:9, 46:10, 46:18,  
 55:13, 55:16, 58:18, 58:19,  
 58:23, 60:14, 60:16, 63:23,  
 64:25.  
 50 64:24.  
 5000 2:36.  
 502 57:1.  
 504 46:22.  
 506--so 46:23.  
 508--i've 48:6.  
 53 48:15.  
 56 24:23.  
 57 24:20.  
 59 58:23, 59:6.  
 .  
 .  
 .  
 < 6 > .  
 6 70:13, 70:15, 70:17, 73:12.  
 60 24:2, 24:13, 64:24.  
 601 70:18.  
 602 70:18.  
 603 70:18.  
 61 68:23, 69:15.  
 64 10:18, 24:1, 27:2, 48:17,  
 58:18.  
 65 68:24, 69:15.

## Concordance

66 11:24, 73:21 .  
 678-5070 2:30 .  
 .  
 .  
 < 7 > .  
 7 5:11 .  
 72 18:5 .  
 747-5070 2:38 .  
 75201 2:37 .  
 75670 1:45, 2:15, 2:43, 2:49 .  
 783-5070 2:23 .

.  
 .  
 < 8 > .  
 8 48:15 .  
 80 27:15 .  
 81 28:9 .  
 82 75:3 .  
 858 2:30 .

.  
 .  
 < 9 > .  
 9 6:11, 18:21, 36:22 .  
 900 2:6 .  
 90067-4276 2:7 .  
 903 1:46, 2:16, 2:44, 2:50 .  
 92130 2:29 .  
 923-7464 2:50 .  
 923-8546 1:46 .  
 923-9000 2:16 .  
 934-8450 2:44 .  
 9:00 1:14 .

---

DATE \_\_\_\_\_ 76:10 .

.  
 .  
 < A > .  
 A. 47:5 .  
 A.M. 1:14 .  
 able 24:16, 26:2, 57:5, 61:21 .  
 ABOVE-ENTITLED 76:3 .  
 absolutely 8:19, 10:17 .  
 abstract 62:25 .  
 access 54:24, 69:21 .  
 accessed 47:23, 47:24 .  
 accomplish 45:1 .  
 accordance 50:17, 66:9, 67:16,  
 67:21, 67:22, 71:2, 71:4, 71:6,  
 71:8, 71:9, 71:12, 71:19 .  
 according 36:13, 49:11, 49:12 .

accused 23:3 .  
 achieved 45:21 .  
 acknowledge 25:1 .  
 acknowledges 67:11 .  
 across 7:6, 12:7 .  
 activated 47:16, 47:20, 47:21 .  
 activating 44:12, 55:9 .  
 active 73:20 .  
 actively 44:21, 46:22, 72:22 .  
 actual 13:25, 35:15, 55:14 .  
 actually 6:13, 7:6, 9:22, 13:16,  
 15:6, 15:11, 18:20, 23:15,  
 36:3, 37:7, 39:1, 41:2, 50:7,  
 58:14, 58:23, 59:22, 59:25,  
 64:21, 71:9, 73:9, 73:10 .  
 added 42:25, 43:6, 43:7 .  
 added. 38:9 .  
 additional 19:12, 34:11, 37:10,  
 57:12, 61:7 .  
 address 28:13, 30:21, 31:9, 38:7,  
 41:4, 42:13, 42:15, 45:11,  
 46:16, 72:8, 74:7, 74:12,  
 74:16, 74:20 .  
 addressed 69:17 .  
 adjourned 75:21 .  
 adjust 23:17 .  
 admissions 35:11 .  
 Admittedly 65:22 .  
 adopted 5:2 .  
 adoption 34:23 .  
 agnostic 16:13 .  
 ago 51:6 .  
 agree 21:16, 32:1, 67:17, 68:16,  
 69:19, 70:24 .  
 agreed 39:13, 39:16 .  
 agreeing 22:18 .  
 agreement 39:1, 39:24, 67:17 .  
 agrees 64:22 .  
 ahead 10:13, 27:13, 57:10 .  
 al 1:12 .  
 Alexsam 21:18, 21:24, 23:1 .  
 Alexsam/cigna 21:7 .  
 alignment 36:23 .  
 ALJ 54:12, 54:14 .  
 allegedly 22:2 .  
 allied 68:25 .  
 allow 34:24, 34:25, 38:18, 47:3,  
 54:7 .  
 allowance 37:21, 37:22 .  
 allowed 37:18 .

allowed--claim 37:18 .  
 allowing 48:13, 48:16 .  
 allows 49:19, 59:4 .  
 already 20:12, 39:13, 51:5 .  
 alter 4:5, 61:23 .  
 altered 39:25 .  
 alternative 11:15, 11:16, 47:13,  
 50:7, 53:20, 73:15 .  
 alternatively 9:19 .  
 ambiguity 40:11, 40:16, 41:10 .  
 amend 4:4, 42:18 .  
 amended 38:7, 41:2, 41:7, 42:1,  
 42:13, 42:24, 43:6 .  
 amending 42:9 .  
 amendment 38:3, 38:16, 38:19 .  
 amount 7:1, 23:15, 24:17, 35:24,  
 36:2, 36:11, 36:16, 36:20,  
 41:6 .  
 amplitudes 9:5, 22:19, 25:2 .  
 amps 24:2, 24:13, 24:14 .  
 analogy 24:6 .  
 analyze 34:5 .  
 Andrews 12:25 .  
 ANGELES 2:4, 2:7 .  
 Annita 2:10, 3:8 .  
 answer 40:3 .  
 answering 56:19 .  
 antecedent 27:17, 27:20, 27:23,  
 28:3, 30:25, 31:2, 32:3 .  
 anticipated 19:5 .  
 anyway 33:2, 56:22 .  
 apologize 44:17 .  
 apparatus 29:1 .  
 appear 5:6, 19:22 .  
 appearances 3:5 .  
 appearing 27:23 .  
 appears 5:11, 13:19, 43:2,  
 56:21 .  
 applicable 15:18 .  
 application 64:5 .  
 applies 22:7, 30:4 .  
 apply 41:9, 42:21 .  
 applying 65:7 .  
 appreciate 5:3, 43:4, 43:15,  
 43:23, 64:14, 64:20, 65:14 .  
 appropriate 3:25, 5:18, 7:1,  
 9:23 .  
 argue 5:3, 27:7, 27:8, 27:12,  
 34:24, 64:11, 67:22 .  
 argued 57:21, 60:12 .

## Concordance

<b>argues</b> 53:22 .	36:10, 36:16, 37:11, 40:23,	<b>buffer.</b> 41:7 .
<b>arguing</b> 53:25, 64:19, 74:3 .	41:6, 65:19, 67:25, 68:8, 72:7,	<b>buffers</b> 44:25, 47:7, 52:9, 52:11,
<b>argument</b> 7:21, 8:13, 9:9, 10:6,	73:8 .	52:17, 52:21, 53:2, 53:7,
10:15, 12:19, 14:20, 14:24,	<b>basic</b> 10:15, 11:3, 25:4 .	56:25, 57:2, 63:23 .
23:7, 25:23, 26:1, 26:24,	<b>basis</b> 4:8, 27:17, 27:20, 27:23,	<b>built</b> 44:16, 54:17, 55:2, 63:9 .
30:12, 32:1, 32:25, 33:13,	28:3, 33:18, 41:19, 46:1 .	<b>bunch</b> 28:16 .
33:19, 34:11, 43:13, 43:15,	<b>becomes</b> 47:17 .	<b>burst</b> 11:10 .
43:21, 59:25, 61:15, 64:13,	<b>before--i'll</b> 39:14 .	<b>Burton</b> 2:32, 3:15 .
67:24, 72:6 .	<b>begin</b> 73:23 .	<b>bus</b> 49:20 .
<b>arguments</b> 4:3, 4:6, 4:8, 42:19,	<b>beginning</b> 65:16, 65:18, 69:16,	<b>byproduct</b> 62:16 .
75:11, 75:18 .	72:17, 72:18, 72:21, 73:1,	<b>byte-wise</b> 72:23 .
<b>around</b> 15:13 .	73:2, 73:17 .	.
<b>array</b> 33:17, 33:25 .	<b>behalf</b> 3:14 .	.
<b>art</b> 5:23, 8:2, 8:9, 8:23, 10:3,	<b>behind</b> 46:2 .	<b>&lt; C &gt; .</b>
11:6, 20:4, 21:3, 49:14, 49:15,	<b>believe</b> 30:15, 34:22, 35:10,	<b>C.</b> 47:12, 58:6 .
49:16, 55:11, 58:18, 59:12,	40:16, 50:13, 71:15, 74:22,	<b>C/A</b> 35:8, 35:16, 35:21, 39:6,
60:19 .	74:23, 75:6 .	39:12 .
<b>art--'dual</b> 5:14 .	<b>believes</b> 41:15 .	<b>CA</b> 2:7, 2:29 .
<b>articulate</b> 11:20 .	<b>Bell</b> 8:18 .	<b>call</b> 47:12, 59:17, 66:24 .
<b>aspect</b> 24:4 .	<b>below</b> 51:3 .	<b>called</b> 45:5, 60:20 .
<b>asserted</b> 62:17 .	<b>best</b> 22:13, 22:21 .	<b>CAMINO</b> 2:28 .
<b>associated</b> 72:23 .	<b>big</b> 38:6, 50:20, 62:5 .	<b>capability</b> 7:21, 12:10, 25:25 .
<b>assume</b> 42:25 .	<b>bit</b> 23:16, 54:12, 66:6, 72:23 .	<b>capable</b> 14:20 .
<b>assumption</b> 12:11 .	<b>blacked</b> 51:25 .	<b>caption</b> 18:21 .
<b>astray</b> 4:4 .	<b>board</b> 13:23, 13:25, 15:21, 17:4,	<b>CAS</b> 75:5 .
<b>Atlantic</b> 8:18 .	17:6, 17:14, 17:16, 28:10,	<b>cases</b> 8:18, 53:24, 55:6 .
<b>attempt</b> 52:14, 52:16, 52:18 .	28:19, 29:3, 29:20, 29:21,	<b>CAUSE</b> 1:5, 53:13, 53:23 .
<b>attention</b> 35:19, 43:24, 64:20 .	29:24, 30:19, 31:8, 32:6, 32:9,	<b>certain</b> 22:19, 44:12, 45:21,
<b>AVE.</b> 2:21 .	33:9 .	59:9 .
<b>AVENUE</b> 2:5, 2:42 .	<b>body</b> 27:18, 27:24, 30:8, 32:21 .	<b>Certainly</b> 19:16, 22:23, 25:14,
<b>aware</b> 46:4 .	<b>bolded</b> 50:11, 50:12 .	28:3, 56:9 .
<b>away</b> 15:25, 32:3, 49:21 .	<b>bottom</b> 10:24 .	<b>CERTIFY</b> 76:1, 76:4 .
<b>awesome</b> 64:12 .	<b>Brief</b> 5:9, 21:7, 25:13, 50:10,	<b>change</b> 38:4, 38:6, 38:17, 38:20,
.	50:11, 50:13, 51:19, 52:6,	38:21, 43:7, 43:9, 51:17 .
.	52:15, 52:25, 57:15, 67:22 .	<b>changed</b> 37:23, 37:24, 42:14,
<b>&lt; B &gt; .</b>	<b>brief--they</b> 68:25 .	67:9 .
<b>B.</b> 46:9, 47:1, 47:14, 47:24,	<b>briefing</b> 4:2, 12:23, 62:5, 67:20,	<b>changes</b> 13:11 .
56:16, 64:1 .	68:4, 75:4 .	<b>changing</b> 38:4, 38:17 .
<b>back</b> 9:2, 9:8, 17:10, 28:9, 31:3,	<b>briefs</b> 13:3 .	<b>character</b> 13:11 .
35:19, 37:23, 38:16, 39:5,	<b>bright</b> 56:8 .	<b>characteristic</b> 9:6 .
39:8, 39:14, 40:1, 42:4, 46:15,	<b>bring</b> 7:13, 15:1, 41:17 .	<b>chart</b> 39:17 .
46:18, 49:25, 50:2, 55:12,	<b>brings</b> 17:20 .	<b>Choi</b> 3:17 .
57:11, 58:15, 64:22, 65:8 .	<b>broad</b> 43:18 .	<b>chose</b> 50:3 .
<b>back--'before</b> 38:5 .	<b>broadest</b> 8:6 .	<b>chosen</b> 74:15 .
<b>backed</b> 74:9 .	<b>brother</b> 27:7 .	<b>circuit--this</b> 24:11 .
<b>bag</b> 25:20 .	<b>buffer</b> 35:25, 44:5, 44:8, 46:21,	<b>circuitry</b> 46:11, 46:19, 63:25 .
<b>bank</b> 49:18 .	46:23, 47:5, 47:15, 52:8, 58:6,	<b>circuits</b> 10:20, 25:8, 26:3, 33:24,
<b>banks.</b> 49:22 .	58:7, 63:4, 63:18, 63:24, 73:9,	34:4, 34:7, 36:23, 47:7, 48:19,
<b>barring</b> 68:9 .	73:15 .	50:17 .
<b>based</b> 4:6, 32:19, 35:11, 35:25,	<b>buffer--'to</b> 45:5 .	<b>circuits"--that</b> 45:5 .

## Concordance

<b>circumvent</b> 55:10 .	17:15, 17:17 .	<b>consistent</b> 14:5, 21:11, 27:18, 37:13, 49:7, 65:10, 68:7, 69:2, 74:25 .
<b>cite</b> 15:8, 21:7 .	<b>command</b> 41:4 .	<b>consistently</b> 8:11 .
<b>cited</b> 19:20, 70:23 .	<b>commission</b> 54:13, 54:15, 54:25 .	<b>constitutes</b> 41:15 .
<b>claimed</b> 30:7, 30:15, 31:11, 31:12, 31:22, 33:2, 33:8, 49:19 .	<b>common</b> 5:16, 42:19 .	<b>constructions</b> 3:22, 3:23, 4:1, 4:5, 4:13 .
<b>Claims</b> 5:11, 13:14, 16:21, 19:23, 22:22, 23:11, 27:18, 37:17, 37:21, 39:24, 41:8, 42:5, 42:8, 42:13, 42:16, 42:24, 43:5, 43:6, 44:15, 49:9, 49:10, 54:3, 54:14, 62:21, 68:5, 72:2 .	<b>communicate</b> 4:20 .	<b>construe</b> 29:11, 32:13, 37:14, 39:1, 39:5, 40:8 .
<b>clarification</b> 33:6, 34:10, 68:9 .	<b>communication</b> 30:3 .	<b>construed</b> 15:22, 41:21, 62:24, 64:2 .
<b>clarity</b> 15:13, 33:13, 35:11, 35:12, 38:8, 42:13, 42:15, 66:6 .	<b>complete</b> 29:1, 60:11 .	<b>construing</b> 38:11, 40:24, 62:12, 67:15 .
<b>clear</b> 10:24, 14:3, 14:6, 20:22, 22:16, 23:14, 29:2, 29:12, 29:16, 30:13, 30:15, 32:15, 33:20, 40:12, 57:24, 65:19, 68:17, 68:25, 69:4, 69:15 .	<b>completed.</b> 73:23 .	<b>contemplated</b> 19:8, 58:15 .
<b>clear--this</b> 52:14 .	<b>completely</b> 6:22 .	<b>contend</b> 55:21, 56:3, 56:15, 74:10 .
<b>clearly</b> 19:23, 32:4 .	<b>complicated</b> 62:21, 63:1, 64:4 .	<b>context</b> 5:23, 6:6, 8:25, 13:13, 16:2, 16:6, 21:3, 21:13, 21:19, 21:23, 22:11, 22:13, 23:2, 23:3, 26:7, 26:9, 28:14, 28:19, 28:20, 29:9, 32:22, 36:5, 39:23, 51:16 .
<b>clock</b> 73:5 .	<b>COMPLY</b> 76:5 .	<b>continuations</b> 62:19 .
<b>closed</b> 47:16, 47:17 .	<b>component</b> 8:22, 12:12, 14:3, 29:6 .	<b>continuing</b> 62:20, 64:5 .
<b>co-counsel</b> 23:17 .	<b>components</b> 6:16, 6:18, 6:20, 7:19, 9:14, 9:15, 10:16, 15:14, 25:17, 27:3, 31:17, 33:10 .	<b>contrary</b> 49:21 .
<b>CO.</b> 1:11 .	<b>components.</b> 7:1 .	<b>contributing</b> 25:7 .
<b>coined</b> 11:6, 51:9 .	<b>comprising</b> 31:14 .	<b>control</b> 28:13, 28:17, 30:21, 31:9, 35:18, 35:21, 41:5, 44:20, 46:10, 46:18, 48:15, 56:25, 57:4, 57:6, 57:7, 57:9, 63:4, 63:6, 63:13, 63:16, 63:25, 68:21, 68:22, 72:20 .
<b>colleague</b> 3:8 .	<b>concede</b> 8:4 .	<b>controller</b> 10:21, 37:1, 48:17, 49:2, 49:6, 58:25, 59:4, 59:8, 59:10, 64:8, 65:13, 69:20, 73:22 .
<b>collection</b> 64:3 .	<b>concept</b> 44:15, 46:8, 48:10, 49:4, 49:9, 51:5, 51:16, 52:3, 52:4, 54:18, 55:2, 55:3, 63:2 .	<b>controller"--and</b> 45:3 .
<b>collision</b> 73:11 .	<b>concern</b> 31:20 .	<b>controller.</b> 45:7, 45:9, 45:19 .
<b>colloquially</b> 44:7 .	<b>concerned</b> 21:25 .	<b>controlling</b> 49:19, 55:6, 70:2, 70:3, 72:16 .
<b>colored</b> 58:5 .	<b>concluded</b> 34:1 .	<b>controls</b> 57:2, 65:17, 68:22, 69:9, 69:24, 73:24, 74:24 .
<b>column</b> 5:20, 6:5, 6:25, 18:21, 19:7, 19:8, 19:19, 48:17, 58:19, 58:23, 59:6, 59:24, 64:24, 64:25, 65:10, 69:15, 69:17, 69:21, 69:22, 74:7, 74:12, 74:20 .	<b>concoct</b> 61:21 .	<b>conversion</b> 29:6, 29:15, 31:16, 33:9 .
<b>columns</b> 58:18 .	<b>condition</b> 46:25 .	<b>converter</b> 5:8, 5:10, 5:14, 5:15, 5:16, 5:25, 6:20, 6:21, 7:5, 7:10, 7:15, 7:22, 8:3, 8:10, 8:20, 9:4, 10:2, 11:5, 11:20, 12:9 .
<b>Colvin</b> 2:39, 3:15, 34:13, 34:15, 34:19, 34:21 .	<b>conduit</b> 29:8 .	<b>converters</b> 6:13, 7:3, 7:6, 7:9, 7:15, 7:16, 7:17, 7:18, 7:19, 7:20, 7:21, 7:22, 7:23, 7:24, 7:25, 7:26, 7:27, 7:28, 7:29, 7:30, 7:31, 7:32, 7:33, 7:34, 7:35, 7:36, 7:37, 7:38, 7:39, 7:40, 7:41, 7:42, 7:43, 7:44, 7:45, 7:46, 7:47, 7:48, 7:49, 7:50, 7:51, 7:52, 7:53, 7:54, 7:55, 7:56, 7:57, 7:58, 7:59, 7:60, 7:61, 7:62, 7:63, 7:64, 7:65, 7:66, 7:67, 7:68, 7:69, 7:70, 7:71, 7:72, 7:73, 7:74, 7:75, 7:76, 7:77, 7:78, 7:79, 7:80, 7:81, 7:82, 7:83, 7:84, 7:85, 7:86, 7:87, 7:88, 7:89, 7:90, 7:91, 7:92, 7:93, 7:94, 7:95, 7:96, 7:97, 7:98, 7:99, 7:100, 7:101, 7:102, 7:103, 7:104, 7:105, 7:106, 7:107, 7:108, 7:109, 7:110, 7:111, 7:112, 7:113, 7:114, 7:115, 7:116, 7:117, 7:118, 7:119, 7:120, 7:121, 7:122, 7:123, 7:124, 7:125, 7:126, 7:127, 7:128, 7:129, 7:130, 7:131, 7:132, 7:133, 7:134, 7:135, 7:136, 7:137, 7:138, 7:139, 7:140, 7:141, 7:142, 7:143, 7:144, 7:145, 7:146, 7:147, 7:148, 7:149, 7:150, 7:151, 7:152, 7:153, 7:154, 7:155, 7:156, 7:157, 7:158, 7:159, 7:160, 7:161, 7:162, 7:163, 7:164, 7:165, 7:166, 7:167, 7:168, 7:169, 7:170, 7:171, 7:172, 7:173, 7:174, 7:175, 7:176, 7:177, 7:178, 7:179, 7:180, 7:181, 7:182, 7:183, 7:184, 7:185, 7:186, 7:187, 7:188, 7:189, 7:190, 7:191, 7:192, 7:193, 7:194, 7:195, 7:196, 7:197, 7:198, 7:199, 7:200, 7:201, 7:202, 7:203, 7:204, 7:205, 7:206, 7:207, 7:208, 7:209, 7:210, 7:211, 7:212, 7:213, 7:214, 7:215, 7:216, 7:217, 7:218, 7:219, 7:220, 7:221, 7:222, 7:223, 7:224, 7:225, 7:226, 7:227, 7:228, 7:229, 7:230, 7:231, 7:232, 7:233, 7:234, 7:235, 7:236, 7:237, 7:238, 7:239, 7:240, 7:241, 7:242, 7:243, 7:244, 7:245, 7:246, 7:247, 7:248, 7:249, 7:250, 7:251, 7:252, 7:253, 7:254, 7:255, 7:256, 7:257, 7:258, 7:259, 7:260, 7:261, 7:262, 7:263, 7:264, 7:265, 7:266, 7:267, 7:268, 7:269, 7:270, 7:271, 7:272, 7:273, 7:274, 7:275, 7:276, 7:277, 7:278, 7:279, 7:280, 7:281, 7:282, 7:283, 7:284, 7:285, 7:286, 7:287, 7:288, 7:289, 7:290, 7:291, 7:292, 7:293, 7:294, 7:295, 7:296, 7:297, 7:298, 7:299, 7:300, 7:301, 7:302, 7:303, 7:304, 7:305, 7:306, 7:307, 7:308, 7:309, 7:310, 7:311, 7:312, 7:313, 7:314, 7:315, 7:316, 7:317, 7:318, 7:319, 7:320, 7:321, 7:322, 7:323, 7:324, 7:325, 7:326, 7:327, 7:328, 7:329, 7:330, 7:331, 7:332, 7:333, 7:334, 7:335, 7:336, 7:337, 7:338, 7:339, 7:340, 7:341, 7:342, 7:343, 7:344, 7:345, 7:346, 7:347, 7:348, 7:349, 7:350, 7:351, 7:352, 7:353, 7:354, 7:355, 7:356, 7:357, 7:358, 7:359, 7:360, 7:361, 7:362, 7:363, 7:364, 7:365, 7:366, 7:367, 7:368, 7:369, 7:370, 7:371, 7:372, 7:373, 7:374, 7:375, 7:376, 7:377, 7:378, 7:379, 7:380, 7:381, 7:382, 7:383, 7:384, 7:385, 7:386, 7:387, 7:388, 7:389, 7:390, 7:391, 7:392, 7:393, 7:394, 7:395, 7:396, 7:397, 7:398, 7:399, 7:400, 7:401, 7:402, 7:403, 7:404, 7:405, 7:406, 7:407, 7:408, 7:409, 7:410, 7:411, 7:412, 7:413, 7:414, 7:415, 7:416, 7:417, 7:418, 7:419, 7:420, 7:421, 7:422, 7:423, 7:424, 7:425, 7:426, 7:427, 7:428, 7:429, 7:430, 7:431, 7:432, 7:433, 7:434, 7:435, 7:436, 7:437, 7:438, 7:439, 7:440, 7:441, 7:442, 7:443, 7:444, 7:445, 7:446, 7:447, 7:448, 7:449, 7:450, 7:451, 7:452, 7:453, 7:454, 7:455, 7:456, 7:457, 7:458, 7:459, 7:460, 7:461, 7:462, 7:463, 7:464, 7:465, 7:466, 7:467, 7:468, 7:469, 7:470, 7:471, 7:472, 7:473, 7:474, 7:475, 7:476, 7:477, 7:478, 7:479, 7:480, 7:481, 7:482, 7:483, 7:484, 7:485, 7:486, 7:487, 7:488, 7:489, 7:490, 7:491, 7:492, 7:493, 7:494, 7:495, 7:496, 7:497, 7:498, 7:499, 7:500, 7:501, 7:502, 7:503, 7:504, 7:505, 7:506, 7:507, 7:508, 7:509, 7:510, 7:511, 7:512, 7:513, 7:514, 7:515, 7:516, 7:517, 7:518, 7:519, 7:520, 7:521, 7:522, 7:523, 7:524, 7:525, 7:526, 7:527, 7:528, 7:529, 7:530, 7:531, 7:532, 7:533, 7:534, 7:535, 7:536, 7:537, 7:538, 7:539, 7:540, 7:541, 7:542, 7:543, 7:544, 7:545, 7:546, 7:547, 7:548, 7:549, 7:550, 7:551, 7:552, 7:553, 7:554, 7:555, 7:556, 7:557, 7:558, 7:559, 7:560, 7:561, 7:562, 7:563, 7:564, 7:565, 7:566, 7:567, 7:568, 7:569, 7:570, 7:571, 7:572, 7:573, 7:574, 7:575, 7:576, 7:577, 7:578, 7:579, 7:580, 7:581, 7:582, 7:583, 7:584, 7:585, 7:586, 7:587, 7:588, 7:589, 7:590, 7:591, 7:592, 7:593, 7:594, 7:595, 7:596, 7:597, 7:598, 7:599, 7:600, 7:601, 7:602, 7:603, 7:604, 7:605, 7:606, 7:607, 7:608, 7:609, 7:610, 7:611, 7:612, 7:613, 7:614, 7:615, 7:616, 7:617, 7:618, 7:619, 7:620, 7:621, 7:622, 7:623, 7:624, 7:625, 7:626, 7:627, 7:628, 7:629, 7:630, 7:631, 7:632, 7:633, 7:634, 7:635, 7:636, 7:637, 7:638, 7:639, 7:640, 7:641, 7:642, 7:643, 7:644, 7:645, 7:646, 7:647, 7:648, 7:649, 7:650, 7:651, 7:652, 7:653, 7:654, 7:655, 7:656, 7:657, 7:658, 7:659, 7:660, 7:661, 7:662, 7:663, 7:664, 7:665, 7:666, 7:667, 7:668, 7:669, 7:670, 7:671, 7:672, 7:673, 7:674, 7:675, 7:676, 7:677, 7:678, 7:679, 7:680, 7:681, 7:682, 7:683, 7:684, 7:685, 7:686, 7:687, 7:688, 7:689, 7:690, 7:691, 7:692, 7:693, 7:694, 7:695, 7:696, 7:697, 7:698, 7:699, 7:700, 7:701, 7:702, 7:703, 7:704, 7:705, 7:706, 7:707, 7:708, 7:709, 7:710, 7:711, 7:712, 7:713, 7:714, 7:715, 7:716, 7:717, 7:718, 7:719, 7:720, 7:721, 7:722, 7:723, 7:724, 7:725, 7:726, 7:727, 7:728, 7:729, 7:730, 7:731, 7:732, 7:733, 7:734, 7:735, 7:736, 7:737, 7:738, 7:739, 7:740, 7:741, 7:742, 7:743, 7:744, 7:745, 7:746, 7:747, 7:748, 7:749, 7:750, 7:751, 7:752, 7:753, 7:754, 7:755, 7:756, 7:757, 7:758, 7:759, 7:760, 7:761, 7:762, 7:763, 7:764, 7:765, 7:766, 7:767, 7:768, 7:769, 7:770, 7:771, 7:772, 7:773, 7:774, 7:775, 7:776, 7:777, 7:778, 7:779, 7:780, 7:781, 7:782, 7:783, 7:784, 7:785, 7:786, 7:787, 7:788, 7:789, 7:790, 7:791, 7:792, 7:793, 7:794, 7:795, 7:796, 7:797, 7:798, 7:799, 7:800, 7:801, 7:802, 7:803, 7:804, 7:805, 7:806, 7:807, 7:808, 7:809, 7:810, 7:811, 7:812, 7:813, 7:814, 7:815, 7:816, 7:817, 7:818, 7:819, 7:820, 7:821, 7:822, 7:823, 7:824, 7:825, 7:826, 7:827, 7:828, 7:829, 7:830, 7:831, 7:832, 7:833, 7:834, 7:835, 7:836, 7:837, 7:838, 7:839, 7:840, 7:841, 7:842, 7:843, 7:844, 7:845, 7:846, 7:847, 7:848, 7:849, 7:850, 7:851, 7:852, 7:853, 7:854, 7:855, 7:856, 7:857, 7:858, 7:859, 7:860, 7:861, 7:862, 7:863, 7:864, 7:865, 7:866, 7:867, 7:868, 7:869, 7:870, 7:871, 7:872, 7:873, 7:874, 7:875, 7:876, 7:877, 7:878, 7:879, 7:880, 7:881, 7:882, 7:883, 7:884, 7:885, 7:886, 7:887, 7:888, 7:889, 7:890, 7:891, 7:892, 7:893, 7:894, 7:895, 7:896, 7:897, 7:898, 7:899, 7:900, 7:901, 7:902, 7:903, 7:904, 7:905, 7:906, 7:907, 7:908, 7:909, 7:910, 7:911, 7:912, 7:913, 7:914, 7:915, 7:916, 7:917, 7:918, 7:919, 7:920, 7:921, 7:922, 7:923, 7:924, 7:925, 7:926, 7:927, 7:928, 7:929, 7:930, 7:931, 7:932, 7:933, 7:934, 7:935, 7:936, 7:937, 7:938, 7:939, 7:940, 7:941, 7:942, 7:943, 7:944, 7:945, 7:946, 7:947, 7:948, 7:949, 7:950, 7:951, 7:952, 7:953, 7:954, 7:955, 7:956, 7:957, 7:958, 7:959, 7:960, 7:961, 7:962, 7:963, 7:964, 7:965, 7:966, 7:967, 7:968, 7:969, 7:970, 7:971, 7:972, 7:973, 7:974, 7:975, 7:976, 7:977, 7:978, 7:979, 7:980, 7:981, 7:982, 7:983, 7:984, 7:985, 7:986, 7:987, 7:988, 7:989, 7:990, 7:991, 7:992, 7:993, 7:994, 7:995, 7:996, 7:997, 7:998, 7:999, 8:000 .
<b>combined</b> 7:15 .	<b>connections</b> 16:23, 16:24, 16:25, 17:17, 18:12, 28:12, 30:20 .	
<b>comes</b> 6:2, 6:3, 13:15, 13:23, 50:2 .	<b>connector</b> 18:19 .	
<b>comfortable</b> 65:11 .	<b>connects</b> 47:11 .	
<b>coming</b> 5:25, 6:1, 6:5, 6:10, 7:5, 9:11, 9:18, 9:19, 9:20, 9:22, 11:21, 15:20, 16:22, 16:23, 16:25, 17:6, 17:10, 17:12, 17:15, 17:17 .	<b>consider</b> 75:19 .	
	<b>consideration</b> 46:5 .	
	<b>considered</b> 27:25 .	



## Concordance

7:12, 9:18, 9:21, 10:1, 11:9, 11:10, 11:11, 13:18, 14:2, 14:12, 14:13, 14:17, 15:21, 16:1, 16:9, 18:11, 19:24, 26:10.	<b>dealing</b> 24:19.	70:16, 70:18.
<b>core</b> 12:4, 44:4, 46:8.	<b>debate</b> 22:8, 22:24.	<b>describing</b> 15:7, 53:19, 55:15.
<b>corporate</b> 3:9, 3:16.	<b>decide</b> 21:14, 21:19, 21:22, 23:1, 23:4.	<b>description</b> 5:20, 8:22, 8:24, 14:4, 18:21, 19:18, 19:22, 20:1, 20:2, 20:5, 25:16, 37:14, 48:3, 49:8, 52:5, 57:24, 67:8, 71:12.
<b>CORRECT</b> 29:14, 38:8, 66:16, 71:16, 76:2.	<b>decides</b> 54:12.	<b>descriptions</b> 6:24.
<b>correctly</b> 67:3, 71:4.	<b>decision</b> 55:2, 55:3, 68:4, 72:1.	<b>designed</b> 4:1, 4:14, 4:17.
<b>corresponding</b> 5:20, 35:8, 35:17, 35:21, 36:4, 38:3, 39:7, 39:12, 41:4.	<b>decisions</b> 21:9.	<b>desirably</b> 45:20.
<b>corresponding'--again</b> 39:6.	<b>default</b> 60:1.	<b>despite</b> 32:20.
<b>correspondingly</b> 63:25.	<b>Defendant</b> 20:17.	<b>detail</b> 6:15.
<b>corresponds</b> 20:6.	<b>DEFENDANTS</b> 1:14, 2:19.	<b>deter</b> 3:23.
<b>Counsel</b> 3:5, 3:21, 4:9, 4:10, 4:21, 14:20, 15:5, 18:9, 18:14, 19:20, 20:2, 33:12, 40:23, 57:21, 57:23, 58:16, 59:20, 60:6, 67:8, 68:10, 68:14.	<b>define</b> 8:24, 28:25, 34:7.	<b>determine</b> 36:23.
<b>couple</b> 28:12, 28:22, 30:20, 45:2, 45:6, 45:12, 61:13.	<b>defined</b> 7:2, 8:11, 8:15, 8:19, 8:20, 8:21, 10:3, 65:9, 71:7.	<b>determined</b> 36:17, 38:21, 40:12, 40:13.
<b>coupled</b> 29:6, 50:18.	<b>defines</b> 5:21, 28:21.	<b>determines</b> 71:21.
<b>coupling</b> 28:20, 29:4, 29:22, 30:22, 30:23, 31:9, 46:2.	<b>definitely</b> 8:21.	<b>determining</b> 35:24, 36:2, 36:20, 37:11, 41:5.
<b>course</b> 6:1, 11:1, 13:2, 13:6, 13:17, 13:22, 14:2, 14:18, 15:17, 24:3, 26:9, 38:11, 38:16.	<b>definition</b> 67:9, 70:23, 74:4.	<b>device</b> 6:7, 28:5, 29:12, 30:14, 30:15, 30:17, 31:22, 31:24, 33:2, 35:18, 35:21, 41:5, 45:8, 46:3, 46:16, 49:2, 50:25, 59:7, 60:22.
<b>Courtroom</b> 64:17.	<b>delay</b> 36:12, 36:13, 36:15, 37:11, 66:20, 66:23, 67:1, 67:4, 67:12, 69:19, 70:22, 70:23, 70:24, 74:9.	<b>device--fpga</b> 6:9.
<b>cover</b> 49:10.	<b>delay--they</b> 66:25.	<b>devices</b> 44:9, 44:12, 44:13, 45:2, 45:6, 45:12, 45:15, 45:18, 47:9, 47:10, 47:23, 49:6, 49:20, 50:19, 53:9, 54:23, 54:25, 59:1.
<b>cranking</b> 14:9.	<b>delay--you</b> 67:1.	<b>devices.</b> 49:1.
<b>crash</b> 53:14.	<b>delaying</b> 73:10.	<b>dictate</b> 71:22.
<b>create</b> 56:9, 65:6, 65:15.	<b>delays</b> 73:10.	<b>dictionary</b> 70:23.
<b>CRR</b> 1:43, 2:47, 76:11.	<b>deleted</b> 51:23.	<b>die</b> 33:17.
<b>crux</b> 13:5, 70:24, 70:25.	<b>deliver</b> 11:12.	<b>DIEGO</b> 2:27, 2:29.
<b>cycle</b> 12:13, 73:12, 73:13.	<b>delivering</b> 10:20.	<b>dies</b> 33:25.
<b>cycles</b> 73:5, 73:14.	<b>DEM</b> 28:15, 28:18.	<b>differed</b> 67:10.
.	<b>demand</b> 10:16, 12:11.	<b>difference</b> 9:15, 32:12.
.	<b>depend</b> 39:22, 71:14.	<b>differently</b> 61:25, 62:2.
<b>&lt; D &gt;.</b>	<b>dependent</b> 5:11, 7:13, 23:14, 71:5, 74:19.	<b>differing</b> 25:6.
<b>D.</b> 50:24, 58:8.	<b>depending</b> 66:13.	<b>difficulty</b> 16:16, 65:7.
<b>DALLAS</b> 2:35, 2:37.	<b>depends</b> 65:5, 66:11, 67:14, 70:10.	<b>direct</b> 46:11, 64:15.
<b>data.</b> 46:12.	<b>depicted</b> 5:13.	<b>directed</b> 19:23, 47:18.
<b>database</b> 21:8, 21:9, 22:1.	<b>depicting</b> 73:12.	<b>directly</b> 14:16, 15:21, 16:8, 17:10, 65:12.
<b>databases</b> 22:2.	<b>depiction</b> 5:12.	<b>disabled</b> 46:24.
<b>DC</b> 2:20.	<b>Deputy</b> 64:18.	<b>disabling</b> 55:22, 56:4, 56:16, 58:11, 59:18, 63:12, 63:25.
<b>deactivating</b> 44:13.	<b>derive</b> 7:23.	<b>disagrees</b> 33:12.
<b>deal</b> 48:5, 50:20.	<b>describe</b> 8:1, 8:3, 24:18, 48:20, 51:23, 52:2, 53:1, 53:3, 53:16, 56:1, 67:12, 70:12, 70:19, 71:10, 75:4.	<b>disclaimed</b> 34:8.
	<b>described</b> 7:17, 8:4, 19:1, 19:6, 44:5, 45:20, 46:7, 52:15, 52:19, 53:18, 58:18, 58:20, 63:16, 67:5, 74:12.	
	<b>describes</b> 6:14, 24:15, 52:3, 53:4, 55:10, 56:18, 63:19,	

## Concordance

<b>disclaimer</b> 33:19, 34:2 .	44:15, 44:23, 55:21, 56:3,	26:4, 37:3, 37:5, 50:7, 50:8,
<b>disclose</b> 50:7, 53:22 .	56:10, 56:15, 57:5, 62:23,	50:17, 51:9, 51:10, 51:18,
<b>disclose"--this</b> 49:17 .	62:24, 62:25, 63:20, 72:22 .	51:21, 52:7, 52:23, 53:20,
<b>disclosed</b> 10:4, 27:4, 56:5, 59:5,	<b>driven</b> 72:10 .	57:22, 59:9, 60:17, 61:22,
59:6, 62:3 .	<b>drives</b> 44:21, 46:22 .	63:14 .
<b>discloses</b> 25:16, 33:24 .	<b>driving</b> 49:11, 50:1, 55:8, 63:17,	<b>embodiments</b> 45:21, 45:23,
<b>disclosure</b> 8:1, 9:10, 13:13, 14:6,	63:19 .	52:12, 53:11, 57:25 .
14:18, 15:2, 19:25, 25:21,	<b>dual</b> 5:8, 5:10, 5:16, 5:25, 6:21,	<b>emphasis</b> 62:5 .
26:7, 26:11, 26:14, 26:15,	7:5, 7:10, 7:15, 8:3, 8:9, 8:20,	<b>emphasize</b> 5:9, 19:18 .
26:20, 50:18, 56:10, 56:11,	10:2, 11:5, 11:10, 11:20, 12:9,	<b>employed</b> 58:1 .
56:12, 56:20 .	56:1 .	<b>enable</b> 46:19, 46:20, 47:14, 52:9,
<b>discuss</b> 50:15 .	<b>duck</b> 56:24 .	63:23 .
<b>discusses</b> 55:8, 66:18, 66:19 .	<b>duration</b> 66:2, 66:13, 66:15,	<b>Enabled</b> 45:2, 45:6, 46:22, 63:11,
<b>discussing</b> 35:16, 48:18, 48:24,	66:24, 67:1, 67:2, 70:10, 72:9,	63:12, 71:19 .
56:11 .	72:14, 72:15 .	<b>enablement</b> 71:22 .
<b>discussion</b> 4:17, 35:24 .	<b>during</b> 35:9, 35:12, 36:17, 36:23,	<b>enabling</b> 49:5, 49:10, 63:12,
<b>displayed</b> 16:15 .	36:24, 37:25, 38:5, 39:10,	63:24, 72:6 .
<b>dispute</b> 13:2, 13:5, 21:13, 21:16,	39:15, 40:4, 40:13, 40:25,	<b>End</b> 27:20, 27:21, 29:13, 30:14,
44:4, 45:23, 50:6, 64:22,	41:12, 42:2, 42:21, 49:14,	65:8, 65:16, 65:18, 66:4,
65:17, 65:24, 67:19, 71:1 .	49:17, 58:24, 59:8, 59:20,	69:10, 69:16, 72:18, 72:21,
<b>disputed</b> 3:22 .	60:3, 60:8, 60:12, 65:7, 72:10,	72:23, 73:2, 73:11, 73:16,
<b>disputes</b> 6:1 .	72:25 .	75:22 .
<b>disputing</b> 5:15 .	.	<b>ends</b> 15:25, 50:23, 50:24, 68:23,
<b>distinct</b> 6:2, 6:9, 20:21, 20:23,	.	69:1, 69:13, 69:25, 70:3,
20:25, 21:1, 21:3, 21:4, 21:5,	<b>&lt; E &gt; .</b>	71:23 .
21:8, 21:11, 21:15, 21:16,	<b>E.</b> 1:44, 2:14, 2:48, 27:8 .	<b>engineering</b> 24:3, 25:4 .
21:20, 22:3, 22:8, 22:10,	<b>earlier</b> 3:20, 35:20, 36:17, 51:7,	<b>Engineers</b> 56:8 .
22:17, 22:18, 23:3, 23:5 .	70:14 .	<b>enough</b> 49:7 .
<b>distinctly</b> 66:17 .	<b>EASTERN</b> 1:2 .	<b>entire</b> 64:3, 69:24, 73:24 .
<b>distinguished</b> 49:14 .	<b>edge</b> 16:23, 16:25, 17:4, 17:7,	<b>equally</b> 22:7 .
<b>distributed</b> 3:21 .	17:11, 17:12, 17:17, 18:9,	<b>equated</b> 40:15 .
<b>DISTRICT</b> 1:1, 1:2 .	18:12, 28:12, 28:16, 30:20 .	<b>equivalence</b> 39:22, 40:2, 40:15,
<b>DIVISION</b> 1:3 .	<b>effect</b> 11:3 .	42:4, 42:5, 43:10 .
<b>Docket</b> 3:4, 75:3 .	<b>efficient</b> 4:11, 20:13 .	<b>equivalent</b> 38:22, 39:9, 39:11,
<b>documents</b> 25:19, 26:19 .	<b>either</b> 3:24, 31:1, 38:12, 41:19,	40:5, 42:6 .
<b>doing</b> 12:10, 14:9, 17:5, 29:21,	46:11, 56:12 .	<b>erased</b> 51:20, 51:22 .
29:22, 29:24, 30:9, 31:8,	<b>EL</b> 2:28 .	<b>errors</b> 38:8 .
45:7 .	<b>elaborate</b> 62:14 .	<b>esoteric</b> 25:3 .
<b>done</b> 13:16, 20:6, 51:22, 61:24,	<b>elapses</b> 66:20, 68:15, 69:19 .	<b>et</b> 1:12, 64:24 .
62:2 .	<b>electrical</b> 24:3, 25:4 .	<b>event</b> 66:20 .
<b>down</b> 10:23, 14:14, 18:1, 33:14,	<b>electrically</b> 45:2, 45:5, 45:14,	<b>events</b> 12:14 .
47:14, 51:3, 68:11, 68:14 .	55:23 .	<b>everyone</b> 64:22 .
<b>down-tick</b> 9:23 .	<b>ELECTRONICS</b> 1:11 .	<b>everything</b> 29:5 .
<b>downscale</b> 9:21 .	<b>element</b> 13:24, 25:4 .	<b>evidence</b> 11:5, 25:18, 71:15,
<b>DRAM</b> 10:21, 10:25, 11:1, 27:3,	<b>elements</b> 12:5, 13:22, 14:8, 33:8,	74:18 .
33:24, 34:4, 34:7 .	48:4, 54:19 .	<b>exact</b> 54:4, 65:14 .
<b>Drams</b> 11:15 .	<b>Ellsberry</b> 49:16, 49:21, 60:1 .	<b>exactly</b> 19:11, 46:7, 55:18,
<b>draw</b> 22:1 .	<b>elmo</b> 64:17 .	71:25 .
<b>drift</b> 75:6 .	<b>embodiment</b> 6:6, 8:2, 11:8,	<b>examination</b> 38:18 .
<b>drive</b> 6:15, 9:13, 44:1, 44:5,	11:14, 11:16, 16:15, 16:17,	<b>example</b> 10:21, 11:13, 12:6,

## Concordance

18:25, 19:6, 23:22, 23:25,  
24:21, 27:19, 29:5, 29:14,  
37:1, 37:18, 46:19, 58:4, 59:6,  
60:20, 63:1, 73:14, 74:14,  
74:15, 74:21 .  
**examples** 36:22, 37:10, 48:14,  
74:15 .  
**Except** 43:17 .  
**excluded** 34:4, 66:15 .  
**Exhibit** 24:25 .  
**experts** 4:18, 21:21, 34:5, 34:6 .  
**explain** 11:23, 37:8 .  
**explanation** 6:4 .  
**express** 74:3 .  
**expressed** 44:12, 67:9 .  
**expressly** 24:15 .  
**extent** 22:19, 39:23, 40:17 .  
**extrinsic** 25:18 .  
.  
.  
**< F > .**  
**F.** 27:10 .  
**faces** 62:11 .  
**fact** 6:11, 15:11, 20:1, 22:2,  
24:11, 30:8, 32:19, 32:20,  
62:11, 65:11 .  
**facts** 55:7 .  
**fail** 42:25 .  
**fails** 57:23 .  
**Fair** 43:3 .  
**fall** 17:3 .  
**falling** 17:15 .  
**falls** 62:1 .  
**familiar** 37:13 .  
**family** 62:18 .  
**far** 16:2 .  
**fear** 15:22, 16:4 .  
**fed** 27:4 .  
**FEDERAL** 23:11, 76:12 .  
**feed** 24:18, 25:7 .  
**feel** 16:7, 66:2 .  
**FEES** 76:4 .  
**felt** 21:13 .  
**few** 5:7, 51:6 .  
**field** 67:7, 67:10, 67:11 .  
**figures** 51:17, 51:20, 52:2, 58:4,  
61:23, 71:11 .  
**final** 7:8, 74:2 .  
**find** 42:16, 43:12 .  
**finding** 16:16, 54:16 .

**finer** 56:23 .  
**fingers** 28:16, 28:17 .  
**finished** 68:4 .  
**first** 4:21, 5:7, 7:9, 9:4, 20:19,  
21:8, 22:4, 22:10, 27:7, 27:21,  
28:10, 29:13, 30:14, 30:16,  
31:12, 31:21, 35:7, 35:24,  
35:25, 41:6, 41:7, 44:21, 45:1,  
64:13, 71:19, 72:17, 72:20,  
72:24, 72:25 .  
**FISH** 2:19, 2:26, 2:34 .  
**fit** 28:11 .  
**five** 9:22 .  
**flash** 10:21, 10:25, 11:15, 27:3 .  
**flashes** 11:1 .  
**fly** 37:9 .  
**focus** 4:3 .  
**focusing** 57:22 .  
**follow** 63:7 .  
**following** 21:18, 22:13, 24:7 .  
**follows** 66:10 .  
**FOREGOING** 76:1 .  
**forgot** 41:1 .  
**fork** 44:7, 44:10, 44:24, 50:22,  
51:13, 51:22, 51:23, 51:25,  
52:1, 53:21, 54:14, 54:15,  
55:1, 55:15, 58:9, 59:17,  
61:16, 61:20, 61:22, 62:22,  
63:3, 63:20 .  
**fork-in-the-road** 51:10, 52:2,  
52:4, 54:4, 55:3 .  
**FORMAT** 76:5 .  
**found** 43:16, 54:3, 54:5, 54:14,  
62:6, 62:18, 70:22, 71:14,  
72:1 .  
**foundation** 9:9 .  
**four** 24:8, 57:24, 57:25, 58:13,  
61:4, 61:5 .  
**fourth** 20:20, 22:5, 23:13 .  
**FPGA** 11:16, 12:1, 12:4, 12:5,  
12:14, 23:23, 26:12, 26:13 .  
**Fpga--and** 11:25 .  
**Fpgas** 12:7, 26:15 .  
**FRANCIS** 2:31 .  
**Frank** 3:15, 35:5 .  
**from--i'll** 38:4 .  
**front** 62:1 .  
**full** 57:22 .  
**function** 45:14 .  
**fundamentally** 22:9 .

**funny** 25:3 .  
.  
.  
**< G > .**  
**gave** 15:15, 23:22, 24:6 .  
**general** 71:13, 74:22 .  
**generally** 74:6 .  
**generated** 13:4, 14:15, 15:15,  
15:20, 15:24, 16:9, 17:16,  
19:4, 36:12 .  
**generating** 13:25, 14:1, 16:25,  
36:12 .  
**gets** 54:13 .  
**getting** 37:17, 39:4, 66:22 .  
**GILLAM** 2:41 .  
**give** 23:22, 34:3 .  
**given** 12:12, 16:2, 65:4, 65:25 .  
**gives** 5:22, 17:8, 32:24 .  
**glad** 62:15 .  
**goals** 60:25 .  
**gold** 28:16, 28:17 .  
**gotten** 71:16 .  
**govern** 4:18 .  
**grammatical** 38:8 .  
**grayed** 58:7 .  
**great** 16:19, 24:10 .  
**green** 15:19 .  
**group** 4:10, 44:14, 48:21, 51:11,  
63:8, 63:21 .  
**grouped** 54:24 .  
**groups** 44:9, 44:12, 45:12,  
45:13 .  
**guess** 16:11, 22:6, 22:19, 25:19,  
25:22, 31:3, 31:19, 32:1,  
32:23 .  
**guidance** 5:19, 34:3 .  
**guides** 32:4, 64:24 .  
**guys** 35:2 .  
.  
.  
**< H > .**  
**half** 35:23 .  
**hand** 22:12, 30:23 .  
**handle** 4:18 .  
**hang** 16:20, 18:14 .  
**happen** 36:3, 41:11, 41:12,  
53:11 .  
**happens** 41:12 .  
**happy** 4:9 .  
**hat** 18:15 .

## Concordance

hear 4:8, 18:1, 18:2, 20:16,  
 57:11.  
**HEARING** 1:22, 3:3, 4:6, 30:12,  
 31:19, 61:17.  
**hearing.** 75:22.  
**height** 23:20.  
**held** 21:10.  
**help** 23:18.  
**helpful** 66:6, 75:19.  
**helping** 37:14.  
**here--before** 37:20.  
**HEREBY** 76:1.  
**herein** 8:21.  
**high** 46:24.  
**higher** 14:9.  
**highest** 22:21.  
**highlighted** 14:7, 35:14, 45:3,  
 45:16, 46:10, 50:14, 65:1.  
**highlighted--and** 48:7.  
**highlighting** 47:8, 51:7.  
**history** 33:19, 33:23, 36:6, 37:7,  
 37:16, 39:8, 40:15, 40:23,  
 41:20, 55:9, 62:4.  
**history--switching** 62:7.  
**Hobbs** 3:10.  
**hold** 30:22.  
**home** 17:20.  
**Honor--i** 56:24.  
**HONORABLE** 1:24.  
**hooks** 16:20.  
**hope** 4:7.  
**host** 28:14, 28:18, 29:4, 29:8,  
 30:24, 30:25, 31:6, 31:24,  
 32:10.  
**HOUSTON** 1:44, 2:14, 2:48.  
 .  
 .  
 < I > .  
**idea** 44:11, 44:19, 45:10, 45:19,  
 47:6, 47:22, 47:24, 48:21,  
 49:8, 50:21, 53:14, 54:18,  
 55:4, 61:24, 62:22, 74:23.  
**identified** 30:14.  
**illustrate** 52:18.  
**illustrated** 18:25, 47:19.  
**illustrates** 49:9.  
**illustrating** 18:22, 18:23.  
**illustration** 36:8, 46:6, 47:2,  
 51:4, 51:13.  
**impact** 32:16.

**impacts** 32:15.  
**impedance** 46:24.  
**implement** 47:24, 50:4, 53:15,  
 55:2.  
**implementation** 54:4.  
**implemented** 61:16, 61:18.  
**implements** 61:20.  
**implication** 8:19, 8:24, 67:23.  
**implicit** 9:5.  
**imply** 71:7.  
**important** 15:17, 46:5, 58:2.  
**in.** 9:20, 73:8.  
**inartful** 72:15.  
**INC.** 1:5.  
**include** 28:12, 31:15, 44:24,  
 67:1.  
**includes** 43:18, 43:19, 66:3,  
 72:18.  
**including** 57:25, 63:4, 71:11.  
**inconsistent** 10:17.  
**increase** 43:9.  
**independent** 7:12, 10:25, 11:17,  
 24:16, 27:5, 52:23, 53:1, 53:3,  
 53:12, 53:16.  
**independently** 11:2, 52:11,  
 52:22, 53:8, 53:17.  
**indicate** 29:23.  
**indulgence** 64:20.  
**informs** 69:20, 73:22.  
**infringe** 62:19.  
**infringement** 54:15, 54:22,  
 65:7.  
**inherent** 70:1, 73:5, 73:7.  
**inherently** 69:11.  
**inhibiting** 48:14.  
**initial** 4:2, 16:11.  
**input** 13:1, 13:6, 13:9, 13:10,  
 13:11, 13:15, 13:17, 13:23,  
 14:1, 14:8, 16:22, 16:24, 17:1,  
 17:2, 17:4, 17:5, 17:11, 17:14,  
 18:8, 18:10, 18:11, 35:7,  
 35:16, 35:21, 36:3, 39:6,  
 39:12, 41:3.  
**inputs** 14:12, 14:17, 48:8.  
**insight** 43:4, 43:14.  
**instance** 7:3, 7:4, 27:7.  
**Instead** 47:19, 61:3.  
**instituting** 68:5.  
**institution** 68:4, 72:1.  
**instructive** 70:15.

**intend** 34:3, 34:7.  
**intended** 4:20, 28:4, 28:6, 28:21,  
 29:19, 30:10, 32:19, 60:23.  
**intention** 68:19.  
**interface** 28:11, 28:15, 28:19,  
 28:22, 29:3, 29:8.  
**interface.** 49:20.  
**interpretation** 41:18, 56:20.  
**interval** 36:13, 36:24, 40:11,  
 40:13.  
**invention** 49:19, 58:15, 58:16,  
 59:3, 59:4, 61:1, 61:16,  
 61:20.  
**inventors** 19:5, 48:2, 58:20.  
**investigation** 53:25, 54:1,  
 54:11.  
**invite** 21:14, 21:17, 22:24.  
**involve** 9:4.  
**involved** 22:3, 54:1, 54:2.  
**IP** 30:1.  
**IPR** 68:3.  
**IRELL** 2:3.  
**irrelevant** 32:3.  
**isolate** 45:11, 45:12, 45:15,  
 45:18, 54:6.  
**isolate"--excuse** 45:17.  
**isolation** 6:7, 46:2.  
**issue** 20:20, 20:23, 21:7, 21:12,  
 21:25, 22:2, 22:4, 25:16, 32:5,  
 34:2, 37:22, 40:19, 41:16,  
 54:13, 54:14, 67:2, 67:4, 68:3,  
 70:25.  
**issued** 42:20, 43:16, 54:6.  
**issues** 4:15, 4:17, 38:7, 42:13,  
 42:15, 68:18.  
**issuing** 3:23.  
**it--""before** 39:14.  
**it--"from** 73:21.  
**it--what** 28:19.  
**italicized** 50:11, 50:13.  
**ITC** 53:24, 62:6.  
**itself** 8:5, 8:6, 11:4, 13:4, 17:8,  
 17:18, 30:15, 40:2, 41:20,  
 67:6, 67:18, 72:19.  
**itself--the** 12:1.  
 .  
 .  
 < J > .  
**Jamie** 3:10.  
**Jason** 2:9, 3:8.

## Concordance

<p> <b>Jayson</b> 3:10.  <b>Jeff</b> 2:32, 3:15.  <b>Jennifer</b> 2:17, 3:6.  <b>JESD</b> 25:20.  <b>job</b> 5:9.  <b>joined</b> 3:14.  <b>joint</b> 39:17.  <b>JUDGE</b> 1:25.  <b>JUDICIAL</b> 64:14, 76:6.  <b>jump</b> 34:25.  <b>jury</b> 21:14, 21:18, 21:22, 22:13, 23:1, 23:4, 23:6.  <b>justified</b> 59:19.  . .  <b>&lt; K &gt; .</b>  <b>keenly</b> 67:3.  <b>kept</b> 61:17.  <b>key</b> 13:16.  <b>kind</b> 44:10, 47:7, 51:18.  <b>known</b> 67:7, 67:11, 74:21, 74:23.  <b>knows</b> 13:2.  . .  <b>&lt; L &gt; .</b>  <b>labeled</b> 46:21.  <b>language--"before</b> 41:3.  <b>large</b> 44:16.  <b>last</b> 64:19.  <b>latency"--that</b> 69:18.  <b>latency"--column</b> 74:16.  <b>later</b> 36:14.  <b>law</b> 20:22, 21:11, 27:22, 37:13.  <b>least</b> 35:25, 41:6, 65:6, 66:11, 67:14, 70:10.  <b>leave</b> 23:5.  <b>Lee</b> 3:18.  <b>left</b> 22:13, 47:8.  <b>left--"and</b> 45:17.  <b>left--"by</b> 45:4.  <b>length</b> 57:21.  <b>less</b> 57:25.  <b>lesson</b> 10:19.  <b>level</b> 9:23, 14:10.  <b>life</b> 32:24.  <b>limitation</b> 16:12, 17:11, 26:5, 27:21, 28:10, 29:13, 30:14, 30:16, 31:12, 31:21, 33:1, 37:4, 41:11, 44:17. </p>	<p> <b>limited</b> 26:18, 40:24, 42:7.  <b>limiting</b> 8:1, 8:12, 26:22, 27:17, 28:2, 28:25, 29:11, 30:6, 30:17, 31:20, 32:13, 32:18, 32:22, 33:7.  <b>line</b> 5:21, 6:25, 10:23, 19:21, 47:4, 49:2, 50:25, 51:8, 51:9, 51:18, 51:21, 52:12, 52:22, 53:11, 53:13, 53:20, 58:10, 58:11, 59:6, 59:16, 61:21, 68:23.  <b>line-drawing</b> 22:8.  <b>lines</b> 11:21, 18:21, 19:7, 22:1, 23:22, 27:5, 50:19, 51:1, 53:10, 58:18, 58:20, 58:22, 58:23, 59:1, 62:7, 64:24, 64:25, 69:15.  <b>lines--one</b> 58:5.  <b>link</b> 70:20.  <b>linked</b> 36:1, 36:21, 69:11, 69:12.  <b>linking</b> 70:21.  <b>litigation</b> 62:17.  <b>little</b> 66:6, 70:14.  <b>LLP</b> 2:3, 2:41.  <b>load</b> 24:4, 24:10, 24:14, 25:7, 48:1, 48:18, 48:20, 50:5, 58:16, 58:21, 58:22, 59:1, 59:7, 59:14, 61:3, 61:4.  <b>load.</b> 59:11.  <b>loads</b> 45:8, 45:10, 46:3, 46:17, 61:4, 61:5.  <b>logic</b> 6:17, 7:16, 8:8, 21:18, 22:7, 22:14, 22:25, 30:4, 44:19, 46:11, 46:19, 63:4, 63:13.  <b>long</b> 15:25.  <b>longer</b> 62:21.  <b>look</b> 5:18, 6:12, 8:8, 11:25, 16:21, 17:20, 18:15, 23:11, 23:25, 24:21, 33:2, 35:14, 36:7, 36:19, 37:7, 44:25, 55:7, 56:24, 58:4, 58:17, 59:24, 64:23, 66:8, 71:9, 72:15.  <b>looking</b> 8:4.  <b>looks</b> 5:12, 28:3, 28:7.  <b>LOS</b> 2:4, 2:7.  <b>lot</b> 53:24.  <b>lots</b> 10:19, 11:8.  <b>lower</b> 45:17.  <b>LTD</b> 1:11.  . </p>	<p> . .  <b>&lt; M &gt; .</b>  <b>M.</b> 2:47.  <b>Madam</b> 64:17.  <b>magic</b> 73:13.  <b>MAGISTRATE</b> 1:25.  <b>MAIN</b> 2:36, 9:9, 10:5.  <b>MAINE</b> 2:21.  <b>management</b> 11:9.  <b>MANELLA</b> 2:3.  <b>marked</b> 46:23.  <b>MARKMAN</b> 1:22.  <b>MARSHALL</b> 1:3, 1:12, 1:45, 2:13, 2:15, 2:43, 2:49.  <b>masking</b> 60:20.  <b>materials</b> 38:15.  <b>Matt</b> 3:15.  <b>MATTER</b> 7:16, 7:17, 37:19, 38:8, 42:25, 43:5, 43:7, 76:3.  <b>matters</b> 16:1, 42:2.  <b>MATTHEW</b> 2:39.  <b>Mckool</b> 2:13.  <b>Mcroberts</b> 1:43, 2:47, 76:9, 76:11.  <b>me--"electrically</b> 45:17.  <b>me--column</b> 48:17.  <b>me--in</b> 46:8.  <b>me--that</b> 54:17.  <b>mean</b> 13:2, 13:8, 15:3, 15:12, 21:20, 22:6, 22:7, 26:7, 29:19, 31:1, 32:1, 32:6, 32:7, 32:14, 36:5, 38:10, 39:23, 42:6, 44:23, 51:17, 56:24, 68:10, 69:9, 71:3, 71:6.  <b>meaning</b> 4:16, 5:17, 5:22, 5:23, 8:23, 16:6, 28:5, 32:24, 41:22, 64:21, 67:10, 67:23, 71:21, 74:23, 75:4.  <b>means</b> 5:23, 21:13, 22:18, 37:8, 39:2, 39:15, 39:18, 40:18, 42:15, 44:19, 56:7, 67:16, 70:2, 71:4, 71:9, 74:19.  <b>meant</b> 42:5, 49:10.  <b>Melissa</b> 2:45, 3:13.  <b>memories</b> 59:13.  <b>mention</b> 41:1, 57:23.  <b>mentioned</b> 37:16, 40:23.  <b>mentions</b> 53:2.  <b>merely</b> 33:24.  <b>merge</b> 53:13. </p>
--	---	---

## Concordance

**met** 16:13.  
**mic** 17:25, 23:17.  
**Michael** 2:11, 2:24, 3:9.  
**microwaves** 24:8.  
**middle** 47:8.  
**Mike** 3:14, 5:5.  
**minor** 38:7, 42:13, 42:15.  
**minutes** 51:6.  
**misrepresentation** 60:12.  
**misunderstanding** 59:22.  
**modified** 55:13.  
**modulated** 13:6, 13:10.  
**modules** 24:18, 31:5, 59:2.  
**moment** 42:1, 65:2, 65:3, 65:12, 69:20, 69:22, 73:1, 73:2, 73:19, 73:22, 73:23.  
**moments** 68:20.  
**morning** 3:1, 3:6, 3:13, 3:14, 3:21, 4:23, 4:24, 5:5, 35:5, 57:11.  
**motivation** 46:2.  
**move** 44:1, 45:14.  
**MS** 2:10, 2:17, 2:45, 3:6, 3:12, 3:13, 3:19, 10:8, 10:11, 10:12, 12:25, 17:24, 17:25, 18:2, 18:4, 19:14, 27:15, 28:7, 29:2, 29:14, 29:17, 33:6, 40:22, 41:24, 57:21, 61:2, 61:7.  
**multiple** 12:2, 22:2, 23:12, 51:1, 51:2.  
**multiplexer** 48:6, 52:7, 52:16, 52:19.  
**myself** 38:15.  
.  
.  
**< N > .**  
**named** 48:2.  
**narrow** 71:3.  
**nature** 22:9.  
**near** 20:2.  
**necessarily** 26:16, 69:11.  
**necessity** 68:23.  
**need** 6:19, 6:21, 7:7, 9:13, 9:25, 19:4, 20:22, 24:13, 25:7, 34:10, 58:9, 59:16.  
**needed** 6:19, 58:9.  
**needs** 13:4, 21:4, 28:22, 29:15, 41:10.  
**new** 38:8, 42:24, 43:5, 43:7, 43:8.  
**next** 12:21, 20:10, 20:13, 64:8.  
**No.** 1:5, 3:3, 18:5, 27:15, 27:19, 28:9, 40:22, 59:24, 60:14, 60:15, 60:16, 71:8.  
**note** 4:12, 11:8, 13:6.  
**notes** 4:13, 4:19.  
**Nothing** 15:2, 26:21, 28:4, 53:4, 57:18, 75:13, 75:16.  
**notice** 37:21, 37:22, 64:14.  
**number** 44:15, 59:3, 73:5.  
.  
.  
**< O > .**  
**object** 10:19.  
**obviously** 16:18, 34:24, 72:14, 72:15.  
**occurring** 32:11.  
**occurs** 16:14.  
**offered** 74:18.  
**Office** 37:23, 38:18, 38:20, 39:14, 42:3, 42:11, 42:22, 42:23, 68:5, 72:1.  
**OFFICIAL** 2:47, 4:14, 76:12.  
**often** 34:25.  
**Okay** 15:9, 29:18, 33:4, 43:11, 45:25, 61:7.  
**ones** 41:2.  
**open** 47:17, 60:24.  
**opened** 60:1.  
**operate** 7:10, 12:2, 12:5, 12:6, 12:7, 52:11, 52:22.  
**operates** 12:1, 13:21, 23:23, 32:4, 57:3, 57:4.  
**operating** 12:12, 12:14, 53:8.  
**operation"--and** 45:16.  
**operation--again** 53:12.  
**operations** 35:10, 35:17, 37:25, 38:6, 38:24, 39:2, 39:10, 39:16, 39:18, 41:1, 41:13, 41:15, 52:8, 54:19, 54:22, 54:24.  
**operations'** 39:3, 39:19, 40:4.  
**operations--or** 53:9.  
**operatively** 50:18.  
**opportunity** 5:3.  
**option** 10:22, 15:15.  
**order** 4:9, 4:15, 4:17, 61:21, 75:20.  
**ordinary** 4:16, 5:16, 8:9, 8:23, 20:3, 32:17, 41:22, 64:21.  
**original** 41:3, 41:11, 66:21, 66:23, 67:19.  
**otherwise** 18:13, 42:21.  
**output** 6:14, 6:19, 6:21, 7:19, 9:13, 14:2, 46:23, 46:24, 48:9, 69:23.  
**outputs** 44:8.  
**outputting** 11:14.  
**outside** 31:6.  
**outstanding** 68:3.  
**overall** 30:17.  
**overcome** 30:5.  
**own** 24:24, 70:23.  
**owner** 11:7, 72:8.  
.  
.  
**< P > .**  
**page** 75:3.  
**paper** 19:13.  
**papers** 5:1, 24:24, 24:25, 27:10, 34:14, 34:17, 34:19, 64:8, 75:7.  
**parameter** 65:6, 66:9, 66:11, 66:13, 66:19, 66:25, 67:12, 67:14, 67:18, 68:8, 68:21, 69:4, 69:8, 69:9, 69:24, 70:11, 71:18, 71:20, 71:21, 72:7, 72:16, 72:20, 72:22, 74:4, 74:6, 74:11.  
**parameters** 24:18, 25:7.  
**parenthetical** 4:19.  
**part** 4:13, 18:17, 18:24, 23:5, 26:13, 29:7, 29:15, 29:23, 29:24, 30:7, 31:12, 31:22, 33:10, 35:20, 68:25.  
**particular** 6:6, 11:25, 12:3, 12:13, 26:12, 27:24, 31:1, 41:14, 57:3, 58:19, 60:2, 60:16, 69:21, 69:22, 74:16.  
**particularly** 7:3, 10:3, 30:9.  
**parties** 69:19.  
**partition** 22:1.  
**parts** 51:23, 57:6.  
**pass** 10:8, 29:9, 39:20, 44:6, 49:5, 55:9, 58:9, 59:21, 60:5, 60:11, 60:17, 60:24.  
**passage** 10:24, 24:11, 27:2, 33:23, 37:2, 68:24, 75:5.  
**passed** 60:5.  
**passes** 60:4.



## Concordance

<b>passing</b> 59:25 .	31:17, 33:9 .	<b>preliminarily</b> 5:2 .
<b>patent--pre-regulated</b> 16:7 .	<b>PNC</b> 24:24 .	<b>preliminary</b> 3:22, 3:23, 3:25, 4:5, 4:12, 8:7, 15:23, 20:25 .
<b>patent--would</b> 53:13 .	<b>podium</b> 39:20 .	<b>premise</b> 9:3, 10:6, 10:15, 11:3 .
<b>patentee</b> 37:23, 38:4, 38:9, 49:14, 50:3 .	<b>point</b> 3:20, 7:8, 7:11, 8:13, 9:15, 10:5, 15:10, 19:21, 21:6, 22:8, 22:16, 25:20, 29:20, 29:25, 30:21, 31:2, 31:5, 32:1, 35:1, 50:14, 53:21, 56:23, 61:14, 64:25, 65:24, 68:19, 72:13, 74:2, 74:5, 75:2 .	<b>PRESCRIBED</b> 76:5 .
<b>patents</b> 48:23, 62:18, 62:20 .	<b>point--the</b> 73:24 .	<b>presentation</b> 6:12 .
<b>patents--excuse</b> 46:8 .	<b>pointed</b> 18:7, 18:10, 20:2, 25:18, 41:9, 53:19, 71:1, 71:4 .	<b>presenting</b> 3:8 .
<b>paths</b> 46:3, 46:13, 46:15, 48:9, 48:11, 48:14, 48:20, 48:22, 49:11, 49:18, 49:20, 49:22, 49:24, 50:1, 50:2, 50:9, 51:2, 52:5, 55:19, 58:13, 60:7, 63:6, 63:12 .	<b>pointing</b> 74:5 .	<b>presumption</b> 30:5 .
<b>PAYNE</b> 1:24 .	<b>points</b> 5:7, 15:5, 61:13, 68:1, 68:12 .	<b>previous</b> 35:10, 36:9, 36:11, 36:17, 36:21, 37:25, 38:6, 38:23, 38:24, 39:2, 39:3, 39:10, 39:15, 39:18, 40:4, 40:13, 40:25, 41:13, 41:14 .
<b>PC</b> 2:19, 2:26 .	<b>portion</b> 18:12, 35:15, 35:19, 64:23 .	<b>previously</b> 47:16 .
<b>PCB</b> 18:25, 19:4, 19:9, 31:11, 31:16 .	<b>portions</b> 50:14, 51:20, 63:10 .	<b>prime</b> 58:1 .
<b>per</b> 58:1 .	<b>position</b> 22:16, 27:16, 33:15, 55:23, 61:9, 69:8, 69:10, 69:14, 70:1, 70:8, 70:13 .	<b>printed</b> 13:22, 28:10, 29:2, 29:3, 29:20, 29:21, 29:24, 30:19, 31:7, 32:6, 32:9, 33:8 .
<b>perceived</b> 48:2, 50:4 .	<b>positions</b> 3:24, 34:23 .	<b>prior</b> 37:12, 49:14, 49:15, 53:24, 55:11, 58:18, 59:12, 60:19, 70:8 .
<b>performing</b> 30:22, 30:23, 45:15 .	<b>possibilities</b> 19:6 .	<b>probably</b> 62:12 .
<b>perhaps</b> 5:2, 66:5 .	<b>possibility</b> 52:20, 61:14 .	<b>problem</b> 45:11, 46:4, 46:16, 47:25, 48:1, 50:4, 58:21 .
<b>period--not</b> 69:25 .	<b>possible</b> 55:24, 57:8 .	<b>problems</b> 53:23, 62:11 .
<b>period.</b> 72:11, 72:25 .	<b>post-allowance</b> 38:19 .	<b>proceed</b> 3:11, 3:18 .
<b>periods</b> 70:18, 70:20, 72:9 .	<b>posture</b> 54:12 .	<b>PROCEEDINGS</b> 76:3 .
<b>permission</b> 27:11 .	<b>power</b> 11:9, 13:24, 14:8, 14:16, 14:24, 14:25, 15:7, 15:20, 17:13, 17:18, 18:16, 18:19, 18:22, 18:23, 19:9, 19:11, 19:18, 24:7, 28:13, 28:17, 30:20, 31:8 .	<b>process</b> 73:13, 73:23 .
<b>personality</b> 23:19 .	<b>powering</b> 7:1 .	<b>product</b> 53:14 .
<b>persuaded</b> 72:5 .	<b>pre-determined</b> 35:24, 36:2, 36:11, 36:16, 36:20, 41:6 .	<b>productive</b> 4:10 .
<b>Petitioner</b> 72:6 .	<b>Pre-regulated</b> 13:1, 13:8, 13:9, 13:11, 13:14, 13:17, 14:1, 14:15, 15:4, 15:18, 15:19, 15:24, 16:12, 16:21, 17:1, 17:5, 17:13, 17:14, 18:8, 18:10, 19:3, 20:7 .	<b>products</b> 54:21 .
<b>phase</b> 65:7 .	<b>pre-regulating</b> 14:10, 14:11, 14:12 .	<b>program</b> 73:8 .
<b>phrase</b> 27:24, 51:9, 63:1, 63:9 .	<b>pre-regulation</b> 15:3, 16:4 .	<b>programmed</b> 73:6 .
<b>physical</b> 28:21, 60:10 .	<b>preamble</b> 27:19, 27:23, 28:24, 29:11, 30:3, 30:17, 31:20, 32:13, 32:24 .	<b>promptly</b> 75:20 .
<b>physically</b> 5:12, 20:25 .	<b>preferred</b> 11:13 .	<b>prong</b> 51:25 .
<b>picture</b> 52:14, 52:15 .		<b>proper</b> 49:5, 74:22 .
<b>piece</b> 13:21 .		<b>proposal</b> 13:6, 13:7 .
<b>pieces</b> 49:15 .		<b>proposed</b> 8:6, 35:9, 44:11, 62:11, 62:14, 65:23, 68:17 .
<b>pink</b> 45:16 .		<b>prosecution</b> 33:19, 33:23, 35:12, 36:6, 37:7, 37:16, 39:8, 40:15, 40:23, 41:20, 42:2, 42:21, 44:23, 49:15, 54:9, 55:9, 59:20, 60:12, 62:3, 62:4, 62:7, 62:20 .
<b>pins</b> 56:10, 69:23 .		<b>prosecution--"disabling</b> 49:18 .
<b>pipes</b> 25:5 .		<b>provide</b> 24:12, 24:13, 28:5, 28:17, 29:9 .
<b>place</b> 18:13, 43:1, 55:15 .		<b>provided</b> 24:2, 35:12 .
<b>placed</b> 24:5, 64:16 .		<b>provides</b> 27:17, 27:20, 27:23,
<b>places</b> 26:11, 51:12 .		
<b>plain</b> 4:16, 41:22, 64:21, 71:20, 74:23 .		
<b>Plaintiff</b> 1:7, 2:3, 3:7, 4:22, 25:23, 30:13, 31:20, 75:16 .		
<b>Please</b> 3:1, 4:25, 10:9, 27:15, 40:22, 57:16, 60:15 .		
<b>pleasure</b> 5:6 .		
<b>plug</b> 24:7, 24:8 .		
<b>plurality</b> 28:12, 29:6, 30:20,		

## Concordance

28:3, 28:14, 28:19, 28:20,  
28:21, 35:10, 36:7 .  
**providing** 29:4, 29:8 .  
**public** 10:5 .  
**pull** 17:25 .  
**purple** 58:5 .  
**purported** 40:2 .  
**purpose** 3:22, 11:7, 58:16 .  
**put** 20:25, 50:11, 52:14, 53:24,  
56:23, 57:7, 62:5, 63:2, 72:4,  
73:21 .  
**puts** 17:19, 50:9 .  
.  
.  
**< Q > .**  
**question** 9:2, 16:19, 22:12,  
22:21, 23:21, 25:22, 36:1,  
38:14, 39:4, 40:3, 43:3, 43:5,  
44:22, 56:2, 56:3, 56:14,  
60:13, 62:2, 62:16 .  
**question--the** 56:24 .  
**questions** 19:12, 20:9, 25:10,  
39:21, 61:8, 62:9 .  
**quibble** 8:14 .  
**quick** 19:15, 41:25 .  
**quickly** 14:22 .  
**quite** 6:15, 15:12, 66:22 .  
**quote** 68:15, 68:24 .  
**quoting** 6:25 .  
.  
.  
**< R > .**  
**rail** 24:1 .  
**rails** 25:5 .  
**Rajan** 33:24 .  
**ran** 12:4, 12:5 .  
**ranges** 12:7 .  
**rank** 51:1, 57:22, 59:5, 59:14,  
69:21, 69:23 .  
**ranks** 47:12, 47:20, 50:24, 57:25,  
58:1, 58:3, 58:6, 58:8, 58:13,  
58:14, 58:19, 59:2, 59:4,  
59:13, 61:17 .  
**ranks.** 50:20 .  
**rather** 3:25, 72:10 .  
**reader** 20:3 .  
**ready** 3:11, 3:18 .  
**REAL** 2:28, 67:4 .  
**real-world** 26:17 .  
**really** 5:21, 8:13, 8:25, 13:5,

13:11, 17:8, 17:19, 17:20,  
18:7, 20:3, 29:19, 30:4, 30:5,  
30:6, 30:9, 30:10, 32:19, 36:1,  
41:17, 41:19, 45:1, 51:12,  
60:2, 64:4, 67:15, 71:1 .  
**reason** 11:19, 12:9, 15:5, 24:7,  
24:9, 25:24, 33:7, 41:9, 46:1 .  
**reasons** 10:19, 11:23 .  
**rebut** 26:1 .  
**receive** 36:14, 48:3, 54:16,  
54:18, 54:19, 54:20, 60:23 .  
**received** 4:6, 18:9, 18:12, 35:25,  
41:6, 54:21, 60:21, 60:22 .  
**receives** 46:19 .  
**receiving** 35:7, 35:16, 35:18,  
35:20, 36:3, 39:6, 39:12, 41:3,  
41:12, 48:4, 53:8 .  
**recess** 57:11 .  
**recess.** 57:15 .  
**recitation** 50:21 .  
**recites** 23:12 .  
**recognized** 59:10 .  
**RECORD** 3:2, 3:5, 3:20, 4:2,  
25:15, 58:1, 64:16, 69:17,  
71:15, 72:5, 72:21, 75:3,  
76:2 .  
**red** 14:7, 52:17 .  
**red--is** 46:24 .  
**redefine** 67:21 .  
**reduce** 45:8, 46:3, 59:7 .  
**reduced** 6:8 .  
**reducing** 47:25, 48:18, 48:20,  
50:2, 61:4, 61:5 .  
**reduction** 58:17, 58:23, 59:14,  
61:3 .  
**redundant** 6:22 .  
**reference** 30:2, 50:8, 52:6 .  
**referenced** 30:8, 32:21, 48:22 .  
**references** 43:19, 48:15, 51:4 .  
**referred** 27:2, 29:13, 44:7 .  
**referring** 31:21, 31:23, 69:18,  
74:11 .  
**refers** 71:18, 74:11 .  
**reflected** 4:15 .  
**regarding** 19:18, 25:19, 42:19,  
43:14, 60:13, 72:1 .  
**Regardless** 59:3 .  
**regards** 43:15, 44:4, 61:14,  
70:17 .  
**regulated** 13:3, 23:12, 23:15 .

**relate** 14:4, 72:9 .  
**related** 17:9 .  
**relates** 35:19 .  
**relevant** 58:22, 65:1 .  
**rely** 8:17 .  
**relying** 55:5 .  
**remark** 41:25 .  
**remarks** 38:3, 57:12, 64:16 .  
**removed** 19:19 .  
**removes** 16:5 .  
**repeated** 49:23, 51:7, 54:8,  
62:17, 62:19, 63:15 .  
**repeats** 51:3 .  
**rephrasing** 70:8 .  
**replace** 52:16 .  
**replaced** 40:4 .  
**replacement** 52:18, 53:1 .  
**reply** 24:25, 52:6, 52:25 .  
**REPORTER** 2:47, 76:12 .  
**represent** 64:11 .  
**representatives** 3:10, 3:17 .  
**represented** 75:7, 75:8 .  
**request** 69:2 .  
**require** 9:16, 10:22, 11:1, 22:22,  
54:15, 58:12, 72:9 .  
**required** 28:12, 30:18, 54:3,  
54:16, 72:19 .  
**requirement** 7:23, 11:11, 11:12,  
12:10, 15:10, 25:25, 32:8 .  
**requirements** 6:17 .  
**requires** 9:7, 23:11, 23:24, 28:7,  
44:6, 67:5 .  
**requiring** 60:2 .  
**reserve** 4:4 .  
**resolve** 69:5 .  
**respect** 20:5, 57:24, 58:20,  
58:24, 60:13 .  
**respective** 72:22 .  
**respond** 14:22, 61:11 .  
**response** 19:15, 25:13, 57:12 .  
**rest** 12:19, 19:10, 19:13, 20:13,  
20:14, 25:9, 27:1, 27:6, 27:9,  
27:10, 28:1, 34:13, 34:16,  
34:19, 41:23, 61:8, 64:7 .  
**restrictions** 18:13 .  
**result** 21:15 .  
**results** 64:4 .  
**retain** 7:14 .  
**retained** 41:3 .  
**reversed** 54:15 .



## Concordance

<p> <b>review</b> 4:2, 54:13.  <b>reviewed</b> 54:14.  <b>reviewing</b> 13:3.  <b>RICHARDSON</b> 2:19, 2:26, 2:34.  <b>right--i'll</b> 52:13.  <b>right--the</b> 19:3.  <b>RMR</b> 1:43, 2:47, 76:11.  <b>road</b> 33:14, 44:8, 44:10, 44:24,              51:14, 51:22, 51:24, 52:1,              53:21, 55:1, 55:15, 58:10,              59:17, 59:18, 61:17, 61:21,              61:22, 62:22, 63:3, 63:20.  <b>route</b> 48:9.  <b>row</b> 69:21.  <b>row.</b> 69:23.  <b>ROY</b> 1:24.  <b>rules</b> 32:17, 38:18.  <b>ruling</b> 30:1.          .          .  <b>&lt; S &gt;.</b>  <b>S/shawn</b> 76:9.  <b>Samsung</b> 1:11, 3:3, 3:14, 3:17,              5:3, 5:5, 18:9, 24:24, 25:18,              33:12, 34:13, 34:19, 34:23,              35:6, 35:9, 41:15, 41:17, 68:6,              70:1, 75:4, 75:13.  <b>SAN</b> 2:27, 2:29.  <b>save</b> 16:10.  <b>saw</b> 51:5, 52:24, 63:5, 63:14,              70:13.  <b>saying</b> 21:2, 25:24, 28:24, 29:10,              32:8, 38:9, 50:21, 55:5, 59:23,              59:25, 64:21, 67:8.  <b>says</b> 15:2, 15:7, 15:8, 15:11,              18:16, 18:22, 27:19, 27:22,              36:12, 41:22, 45:7, 48:7,              49:16, 51:16, 52:21, 53:17,              59:7, 61:19, 65:12, 67:6,              73:19, 73:21.  <b>scheme</b> 57:4.  <b>scope</b> 15:23, 32:16, 38:17,              38:20, 38:21, 39:25, 42:24,              43:9.  <b>screen</b> 9:3, 59:15, 75:6.  <b>seated</b> 3:1, 57:16.  <b>second</b> 6:8, 13:20, 19:9, 20:20,              21:8, 22:10, 35:23, 44:22,              45:14, 46:23, 58:6, 58:11,              59:16, 59:18, 60:17, 67:2,       </p>	<p>         68:18, 72:24, 73:1.  <b>seconds</b> 24:2, 24:13.  <b>section</b> 15:6, 44:21, 50:12, 65:1,              72:23.  <b>seeing</b> 57:9.  <b>seeking</b> 39:1, 39:5, 40:8, 66:2.  <b>seem</b> 33:12.  <b>seemed</b> 67:21.  <b>seems</b> 40:8, 67:17, 71:1, 71:6,              74:3.  <b>seen</b> 44:20, 45:8, 51:19, 59:7,              62:13.  <b>sees</b> 58:25, 59:2, 59:13.  <b>select</b> 44:13, 48:8.  <b>selected</b> 49:6, 60:21, 69:21,              69:23.  <b>selecting</b> 46:13, 48:16, 50:1,              59:21, 60:6.  <b>selection</b> 46:14, 46:15, 46:16,              46:25, 48:10, 48:13, 55:10.  <b>selectively</b> 48:13, 48:22, 48:25,              54:6, 54:8.  <b>selects</b> 46:11, 48:8.  <b>send</b> 6:20, 46:12.  <b>sense</b> 7:16, 8:20, 25:24, 58:12.  <b>sent</b> 60:21.  <b>sentence</b> 50:23, 50:24.  <b>separate</b> 6:9, 7:11, 7:12, 7:14,              9:10, 10:16, 10:20, 11:15,              18:11, 18:19, 21:1, 21:4,              23:21, 25:1, 26:4, 27:3, 27:4,              31:5.  <b>seq</b> 64:24.  <b>serial</b> 62:20, 64:5.  <b>serve</b> 13:17, 60:25.  <b>set</b> 3:21, 16:22, 54:25, 69:5,              69:8.  <b>sets</b> 47:9, 47:11.  <b>SHAWN</b> 1:43, 2:47, 76:11.  <b>shawn_mcroberts@txed.uscou</b>              <b>rts.gov</b> 1:47.  <b>shift</b> 14:14.  <b>short</b> 24:9.  <b>shouldn't</b> 15:9.  <b>show</b> 59:15.  <b>showed</b> 51:5, 63:23.  <b>showing</b> 47:6.  <b>shown</b> 18:24.  <b>shows</b> 5:11, 26:4, 46:7, 51:13,              52:12.       </p>	<p> <b>side</b> 3:24, 14:21, 22:1, 44:21,              44:22, 48:3, 49:12, 63:17,              63:18, 63:20, 72:24, 72:25,              73:1.  <b>sided</b> 68:6.  <b>sides</b> 3:21.  <b>signal</b> 36:10, 36:13, 36:14,              36:15, 46:20, 49:12, 55:22,              56:3, 56:15.  <b>signal.</b> 46:19.  <b>signals</b> 15:14, 26:21, 28:13,              28:18, 28:22, 29:4, 29:9,              30:21, 31:9, 35:8, 35:16,              35:21, 35:25, 36:3, 39:6,              39:12, 41:4, 41:6, 48:15.  <b>significant</b> 65:6.  <b>similar</b> 22:4, 37:20, 48:3, 62:18.  <b>simple</b> 62:22.  <b>simply</b> 41:8.  <b>single</b> 7:4, 10:23, 21:25, 36:22,              49:1, 51:8, 51:16, 53:10,              53:11, 58:3, 58:9, 59:5, 59:11,              59:14, 59:16, 60:8, 62:1,              62:14, 64:2.  <b>sir</b> 57:20.  <b>sit</b> 35:1.  <b>sitting</b> 32:6, 32:9.  <b>situation</b> 30:2, 30:11, 32:18,              32:20.  <b>situations</b> 26:18.  <b>skill</b> 8:9, 20:4.  <b>sky</b> 17:3, 17:15.  <b>Slide</b> 5:11, 6:11, 11:24, 14:23,              18:5, 23:2, 24:20, 24:23,              27:15, 28:9, 40:22, 55:13,              59:24, 60:15, 70:14.  <b>slides</b> 10:8, 12:25, 37:9, 51:7.  <b>slot</b> 28:11.  <b>Smith</b> 2:13, 2:41, 2:45, 3:13,              3:19, 10:8, 10:11, 10:12.  <b>Sohi</b> 3:10.  <b>Sol</b> 30:1.  <b>solution</b> 48:1, 50:3, 50:4.  <b>solve</b> 47:25.  <b>solved</b> 46:4.  <b>somehow</b> 52:11, 53:19.  <b>Sometimes</b> 44:7, 52:10.  <b>Sorry</b> 58:21.  <b>sorry--data</b> 53:9.  <b>sort</b> 9:9, 13:21, 21:17, 68:18.       </p>
---	--	--

## Concordance

<b>sought</b> 66:12 .	74:12, 74:17, 74:20 .	<b>terminal</b> 47:18 .
<b>sounds</b> 7:20 .	<b>structural</b> 17:11 .	<b>terminals</b> 48:5, 55:20 .
<b>source</b> 8:13, 13:15, 14:24, 14:25, 15:7, 17:16, 17:18 .	<b>structure</b> 17:9, 17:19, 28:22 .	<b>terms</b> 3:22, 3:25, 4:18, 18:13, 20:17, 21:5, 26:20, 32:14, 37:15, 38:10, 38:12, 38:25, 40:15, 42:3, 44:2, 44:5, 44:23, 75:12 .
<b>sources</b> 15:20 .	<b>struggling</b> 22:22, 26:4 .	<b>test</b> 27:17 .
<b>SOUTH</b> 2:42 .	<b>stuck</b> 10:4 .	<b>TEXAS</b> 1:2, 1:12, 1:45, 2:15, 2:37, 2:43, 2:49 .
<b>spatial</b> 60:10 .	<b>subject</b> 37:19 .	<b>text</b> 27:24, 32:21, 46:10 .
<b>speaking</b> 24:11 .	<b>subsequent</b> 36:25, 65:15 .	<b>Tezyan</b> 2:11, 3:9, 64:10 .
<b>spec</b> 63:14 .	<b>sudden</b> 32:7 .	<b>that--"is</b> 69:19 .
<b>specialized</b> 11:6 .	<b>sufficient</b> 58:3, 59:16, 71:25 .	<b>that--but</b> 43:15 .
<b>specific</b> 26:20, 40:9, 42:18, 60:3, 60:9, 67:8, 67:23, 74:6, 74:20 .	<b>sufficiently</b> 72:5, 72:8 .	<b>that--makes</b> 68:25 .
<b>specifically</b> 15:16, 29:23, 38:7, 51:4, 52:3, 55:1 .	<b>suggest</b> 59:18 .	<b>that--where</b> 37:18 .
<b>specification--switching</b> 49:24 .	<b>SUITE</b> 2:6, 2:14, 2:21, 2:36 .	<b>the--excuse</b> 54:17 .
<b>spirit</b> 4:7 .	<b>superfluous</b> 6:22, 7:7, 9:11, 9:12 .	<b>themselves</b> 52:2 .
<b>split</b> 52:8, 54:23, 55:16 .	<b>supplied</b> 10:23, 11:2 .	<b>they've</b> 15:22, 51:19, 51:22 .
<b>splitting</b> 63:6 .	<b>supply</b> 10:25, 11:4 .	<b>thinking</b> 8:9 .
<b>ST.</b> 2:14 .	<b>support</b> 16:15 .	<b>third</b> 7:9, 9:4, 20:20, 22:10 .
<b>stand</b> 5:1, 12:23 .	<b>supports</b> 20:8 .	<b>though</b> 4:16, 24:16, 30:8, 31:2, 54:3, 57:24 .
<b>standard</b> 11:12 .	<b>supposed</b> 28:17 .	<b>three</b> 20:13, 24:18 .
<b>STARS</b> 2:5 .	<b>SW</b> 2:21 .	<b>throughout</b> 12:12, 27:18, 71:10 .
<b>start</b> 12:8, 18:5, 18:6, 23:10, 36:8, 65:5, 66:3, 66:10, 66:12, 67:14, 69:5, 69:9, 69:12, 70:9, 71:5, 72:10, 73:11, 73:16 .	<b>swapped</b> 40:5 .	<b>thrust</b> 35:18, 35:23 .
<b>started</b> 29:19 .	<b>switch</b> 17:24, 44:9 .	<b>tied</b> 14:16, 14:18, 15:21, 16:8, 17:9 .
<b>starting</b> 5:21, 59:6 .	<b>switched</b> 60:8 .	<b>time--but</b> 67:1 .
<b>starts</b> 37:3, 40:6, 58:23, 63:3, 65:2, 65:13, 68:8, 68:22, 69:1, 69:25, 70:2, 71:22, 72:7 .	<b>switches</b> 48:25, 49:1, 49:19, 60:1 .	<b>time--right</b> 66:20 .
<b>state</b> 3:5, 47:2 .	<b>switching</b> 44:6, 46:2, 48:18, 48:19, 48:20, 48:22, 49:3, 49:9, 49:22, 50:1, 50:9, 52:5, 59:21, 60:6, 60:7, 60:11, 62:5, 63:3, 63:7 .	<b>time--which</b> 66:23 .
<b>statement</b> 28:4, 42:7, 42:22, 42:23, 66:1 .	<b>systems</b> 15:25, 25:19, 31:10 .	<b>Tobin</b> 3:10 .
<b>statements</b> 65:25 .	.	<b>today</b> 3:7, 3:9, 75:17 .
<b>STATES</b> 1:1, 1:25, 23:23, 76:7 .	.	<b>today--young-jun</b> 3:17 .
<b>stay</b> 12:12 .	<b>&lt; T &gt; .</b>	<b>together</b> 7:13, 13:21, 14:19, 17:19, 53:14, 70:20 .
<b>STE</b> 2:28 .	<b>talked</b> 12:3, 13:18, 14:13 .	<b>took</b> 42:14, 57:6, 73:14 .
<b>step</b> 16:2, 41:10, 41:12 .	<b>talks</b> 12:13, 24:1, 27:3, 37:11, 47:13, 49:4, 63:17, 63:22, 66:19, 71:17 .	<b>tools</b> 11:9 .
<b>steps</b> 36:8 .	<b>taller</b> 23:16 .	<b>top</b> 31:4, 46:20, 46:21, 55:16 .
<b>stock</b> 51:12, 53:24 .	<b>targeted</b> 49:6 .	<b>top--"to</b> 45:8 .
<b>stops</b> 65:3, 65:13 .	<b>teaches</b> 49:21 .	<b>tough</b> 43:21 .
<b>straight</b> 33:22, 51:9, 51:18, 51:21, 52:12, 52:22, 53:11, 53:20, 58:10, 61:21 .	<b>technically</b> 69:10 .	<b>TRANSCRIPT</b> 76:2, 76:4 .
<b>strange</b> 51:18, 54:12 .	<b>technique</b> 60:20 .	<b>transmission</b> 36:25, 45:4, 47:3, 47:7, 48:16, 48:25, 50:16, 59:9 .
<b>STREET</b> 1:44, 2:36, 2:48 .	<b>technology</b> 7:17, 21:23, 22:11, 62:18 .	<b>triggers</b> 24:4 .
<b>strip</b> 24:8 .	<b>technology--you</b> 21:19 .	<b>tristate</b> 46:21, 46:23, 47:4, 47:15, 52:8, 52:10, 52:17, 52:21, 53:1, 53:7, 56:25, 57:2, 63:22, 63:24, 73:9, 73:15 .
<b>strobe</b> 36:10, 36:16, 69:17, 74:7,	<b>tells</b> 20:3 .	
	<b>temporal</b> 60:9 .	
	<b>tentative</b> 66:14 .	
	<b>term-by-term</b> 4:8 .	

## Concordance

**true** 42:22, 43:1, 43:8.  
**Truelove** 2:17, 3:6, 3:7, 3:12.  
**try** 34:7, 44:18, 52:14, 75:19.  
**trying** 41:17, 47:25, 67:21, 68:16.  
**tuned** 66:18, 67:3.  
**turn** 4:21, 14:1, 14:13, 20:10.  
**turned** 47:16, 60:3, 60:5, 60:18, 60:19.  
**turning** 60:10.  
**turns** 46:20.  
**two-rank** 58:21, 58:24, 59:12, 59:15, 61:15.  
**type** 74:6, 74:16.  
**types** 6:15, 11:8.  
 .  
 .  
**< U > .**  
**ultimately** 21:22, 22:11, 23:4, 63:7.  
**unclaimed** 31:23.  
**unclear** 40:7.  
**uncommonly** 4:5.  
**undergone** 64:5.  
**understand** 16:14, 22:20, 23:7, 25:23, 26:23, 33:15, 34:1, 34:2, 34:9, 61:9, 64:4, 68:17, 70:7.  
**understanding** 16:16, 60:18, 66:1, 66:6, 66:14, 66:16, 71:20, 73:3.  
**Understood** 5:17, 5:22, 33:1, 33:21, 59:20, 67:20.  
**unfortunately** 62:16.  
**uniform** 49:8, 52:4.  
**uniquely** 8:11.  
**UNITED** 1:1, 1:25, 76:7.  
**unless** 20:9, 25:9, 39:21, 62:8.  
**unlimiting** 27:25.  
**unnecessary** 6:22.  
**until** 73:16, 73:23.  
**useful** 26:1, 60:22.  
**uses** 70:18.  
**using** 25:17, 45:4, 61:16, 69:5, 69:7, 69:8.  
 .  
 .  
**< V > .**  
**value** 7:4, 7:5, 7:18, 7:22, 9:15, 9:20, 9:21, 9:23, 10:16, 21:4,

46:22, 52:9, 52:10.  
**values** 6:13, 7:12, 7:14, 7:24, 9:10, 9:12, 9:16, 9:24, 21:5, 26:21.  
**variable** 71:7.  
**variety** 4:12.  
**various** 7:1, 26:10, 29:21, 71:10.  
**version** 55:13, 55:14.  
**versus** 3:3, 38:24, 63:8.  
**view** 8:6, 32:25.  
**Voila** 51:21.  
**voltages** 5:25, 6:1, 6:10, 12:2, 12:10, 12:14, 13:17, 17:1, 17:2, 17:4, 17:5, 17:9, 17:12, 17:14, 22:5, 22:10, 23:12, 23:13, 23:15, 23:24, 24:16, 25:1, 25:6, 25:25, 26:2, 26:5.  
**volts** 6:19, 9:22, 10:22, 11:2, 11:14, 12:8, 24:2, 24:8, 24:12, 27:4.  
**vs** 1:9.  
 .  
 .  
**< W > .**  
**wading** 64:21.  
**walk** 13:20, 46:6.  
**wanted** 4:19, 9:14, 22:15, 66:25.  
**wants** 22:1, 34:23, 40:17.  
**WASHINGTON** 2:20, 2:22, 2:42.  
**well-established** 27:22.  
**Whatever** 3:24, 4:9, 35:1, 41:8.  
**whereas** 6:7.  
**Whereby** 46:10.  
**wherein** 65:5, 66:10.  
**wherever** 42:12.  
**whether** 13:3, 22:3, 22:9, 23:1, 23:2, 29:12, 29:14, 32:24, 41:14, 44:5, 50:6, 50:7, 60:16, 67:8, 68:10, 72:8.  
**whole** 6:7, 63:1, 69:5, 73:24.  
**wide** 72:23.  
**wire** 24:1.  
**wireless** 30:3.  
**wires** 11:3.  
**with--just** 26:4.  
**within** 7:5, 8:7, 30:8, 30:16.  
**Without** 28:24, 33:11, 55:22, 56:4, 56:16, 59:17, 61:22.  
**Won-jin** 3:18.

**word** 8:15, 13:8, 20:7, 51:16, 55:1, 62:12, 62:23, 64:2, 72:14.  
**words** 54:19, 55:22, 62:13.  
**work** 42:10, 53:7, 53:23.  
**write** 36:9, 36:10, 36:23, 37:12, 44:18, 58:25, 59:8, 60:4, 60:20, 60:23, 72:23, 73:13.  
**written** 16:13, 68:11.  
**wrote** 68:14.  
 .  
 .  
**< Y > .**  
**Y1** 47:5, 48:4, 52:9, 53:10, 55:20.  
**Y2** 47:18, 48:5, 53:10, 55:20.  
**Y2.** 52:10.  
**yellow** 45:4.  
**yesterday** 24:6, 64:12.  
**you--that** 62:1.  
 .  
 .  
**< Z > .**  
**Zheng** 3:10.  
**ZHONG** 2:10, 3:8, 17:24, 17:25, 18:2, 18:4, 19:14, 24:6, 27:15, 28:7, 29:2, 29:14, 29:17, 33:6, 40:22, 41:24, 57:21, 61:2, 61:7.